

# Compal Confidential

DIUYA/YB/SA/SB/SD (KBL-R)

DIS M/B Schematics Document

Intel KabyLake U/KabyLake R Processor with DDR4

N16S-GTR(940) (23x23mm)

N16V-GMR1(920) (23x23mm)

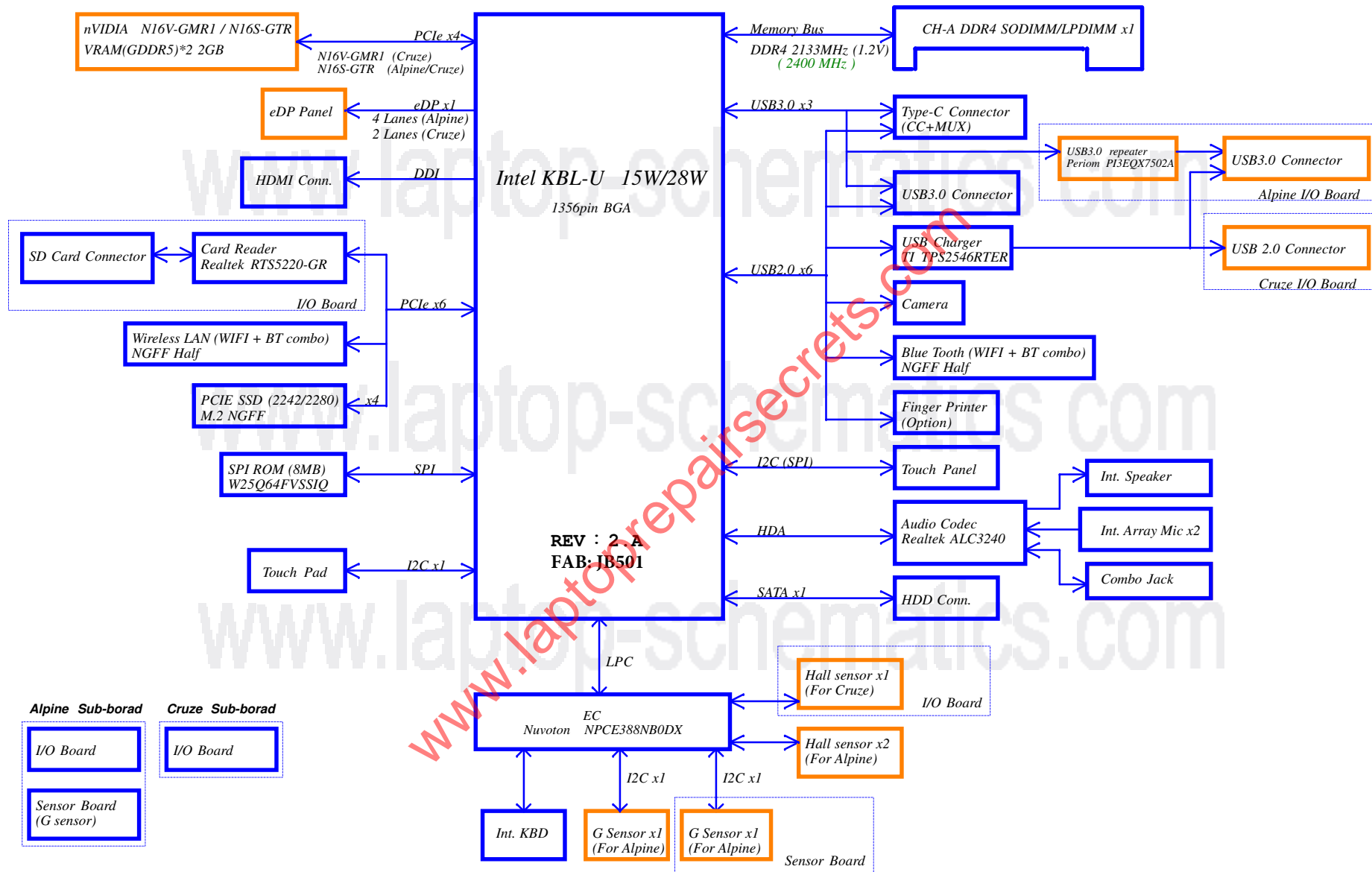
2017-06-05

LA-E541P

REV : 2.A

FAB: JB501

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				Custom	LA-E541P	2A
Date: Wednesday, June 21, 2017				Sheet	1	of 51



# Voltage Rails

State	power plane	B+	+5VALW	+1.2V	+5VS +3VS +1.35VS +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.6VS +1.0VALW
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

# BOM Structure Table

Item	BOM Structure
For DIS	DIS@
For UMA	UMA@
For Touch Panel with SPI	TS_SPI@
For Touch Panel with I2C	TS_I2C@
For Keyboard backlight	KBL@
No Keyboard backlight	NOKBL@
For Samsung VRAM	S2G@
For Micron VRAM	M2G@
For Hynix VRAM	H2G@
For UHD Panel	UHD@
For Finger Printer	FP@
For SSD	SSD@
For EMI	EMI@
For ESD	ESD@
For RF	RF@
No EMI	@EMI@
No ESD	@ESD@
No RF	@RF@
Connector	ME@
For VARM X76	X76@
For Test Point	TP@
For Debug	@DCI@
For S series only	S_AL@
For S IMR series only	S_IMR@
For YOGA series only	YOGA@
For CPU Type	17_7500U_R1@ 15_7200U_R1@ i3_7100U_R1@ i7_7500U_R3@ i5_7200U_R3@ i3_7100U_R3@ pt_4415U_R1@ pt_4415U_R3@ i3_6006U_R3@

Item	BOM Structure
For KBL U22 CPU	U22@
For KBL U42 CPU	U42@
For GPU Type	N16S_R1@ N16S_R3@ N16V_R1@ N16V_R3@
For EMI	U22_EMI@ U42_EMI@
For Thermal sensor	EX_THM@
For ESD	FP_ESD@

# USB 2.0 Port Table

Port	External USB Port
1	USB3 Type-C Port
2	USB2/3 Port (MB)
3	USB2/3 Port (IO/B)
4	USB3 Type-C Port
5	Camera
6	Finger Printer (Option)
7	NGFF WLAN+BT

# USB 3.0 Port Table

Port	External USB Port
1	USB3 Type-C (MUX)
2	USB2/3 Port (MB)
3	USB2/3 Port (IO/B)
4	
5	
6	

# SATA Port Table

Port	External SATA Port
0	HDD
1	

# PCIe Port Table

Lane	Port	External PCIe Port
1		
2		
3	1	GPU
4		
5		
6		Card Reader
7		NGFF WLAN+BT
8		
9		
10		
11	3	SSD
12		

# EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h
Device NCT7718W	
Device 1001 100x 98h	

# EC SM Bus2 address

Device	Address
BMA250E	0001 100x 18h

# PCH SM Bus address

Device	Address
DOR_JDIMM1 Touch Pad	1010 000x A0h

# GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

# SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	DGPU			TP	PCH	G-SENSOR
SMB_EC_CK1	NECP388	✗	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW	+19V_VIN									
SMB_EC_CK2	NECP388	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SMB_EC_DA2	+3VS		+3VGS										
SMB_EC_CK4	NECP388	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SMB_EC_DA4	+3VALW												
PCH_SMBCLK	PCH	✗	✗	✗	✗	✓	✗	✗	✗	✓	✗	✗	✗
PCH_SMBDATA	+3VALW												
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✗	✗
SML0DATA	+3VALW												
SML1CLK	PCH	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SML1DATA	+3VALW												

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

# X4E

# Yoga Series

ZZZ4 X4E_YA@	ZZZ3 X4E_YA_FP@	ZZZ5 X4E_YB@	ZZZ6 X4E_YB_FP@
X4E Y Series X4EASR38L1	X4E Y Series FP SKU X4EASR38L2	X4E Y Series UHD SKU X4EASR38L2	X4E Y Series UHD+FP SKU X4EASR38L1

# S Series

ZZZ7 X4E_S@	ZZZ7 X4E_S_FP@
X4E S Series X4EASR38L1	X4E S Series FP SKU X4EASR38L2

# HDMI Logo

ZZZ 45@
HDMI Logo RC0000003HM

# Yoga Series (U42)

ZZZ X4E_U42_YA@	ZZZ X4E_U42_YA_FP@	ZZZ1 X4E_U42_YB@	ZZZ2 X4E_U42_YB_FP@
X4E Y Series X4EASR38L2	X4E Y Series FP SKU X4EASR38L1	X4E Y Series UHD SKU X4EASR38L2	X4E Y Series UHD+FP SKU X4EASR38L1

# S Series (U42)

ZZZ X4E_U42_S@	ZZZ X4E_U42_S_FP@
X4E S Series X4EASR38L1	X4E S Series FP SKU X4EASR38L2

# PCB part

ZZZ YOGA@
PCB Y Series DA80019512A
ZZZ S_AL@
PCB S Series DA80019512A
ZZZ S_IMR@
PCB S Series DA80019512A

# GDDR5 VRAM \* 2

# X7671138L03

U6 S2G@	U7 S2G@
K4G80325FB-HC03 SA000094R20	K4G80325FB-HC03 SA000094R20
RV65 SDQ34499180 1.99K_0402_1% S2G@	RV65 SDQ34499180 1.99K_0402_1% S2G@

# X7671138L02

U6 M2G@	U7 M2G@
MT51J256M32HF SA000096R20	MT51J256M32HF SA000096R20
RV65 SDQ34499180 1.99K_0402_1% M2G@	RV65 SDQ34499180 1.99K_0402_1% M2G@

# X7671138L01

U6 H2G@	U7 H2G@
H5GCB824MJR-T2C SA000092G10	H5GCB824MJR-T2C SA000092G10
RV65 SDQ34499180 30.1K_0402_1% H2G@	RV65 SDQ34499180 30.1K_0402_1% H2G@

# GPU part

U1 N16S_R1@	U1 N16V_R1@
N16S-GTR-S-A2 BGA 595P SA000097P00	N16V-GMR1-S-A2 BGA 595P SA000097T00
U1 N16S_R3@	U1 N16V_R3@
N16S-GTR-S-A2 BGA 595P SA000097P00	N16V-GMR1-S-A2 BGA 595P SA000097T00

# CPU part

# KBL U22 (= U22@)

U1 i3_7100U_R1@	U1 i5_7200U_R1@	U1 i7_7500U_R1@	U1 i7_4415U_R1@
QLYKH0 2.4G SA0000A38A0	QLYYH0 2.5G SA0000A37A0	QLYYH0 2.7G SA0000A37A0	QLYYH0 2.9G SA0000A37A0
U1 i3_7100U_R3@	U1 i5_7200U_R3@	U1 i7_7500U_R3@	U1 i7_4415U_R3@
SR343 H0 2.4G SA0000A38B0	SR342 H0 2.5G SA0000A37B0	SR341 H0 2.7G SA0000A34A0	SR348 H0 2.9G SA0000A37A0

# SKL U22 (= U22@)

U1 i3_6006U_R3@
SR2JG R1 i3_6006U 2.0G C381 SA0000ACN10

# KBL U42 (= U42@)

U1 i5_QNFB_R1@	U1 i7_QNFB_R1@
QNEF Y0 1.6G FCBGA SA0000AWB00	QNEF Y0 1.6G FCBGA SA0000AWC00
U1 i5_QNFB_R3@	U1 i7_QNFB_R3@
QNEF Y0 1.6G FCBGA SA0000AWB50	QNEF Y0 1.6G FCBGA SA0000AWC50

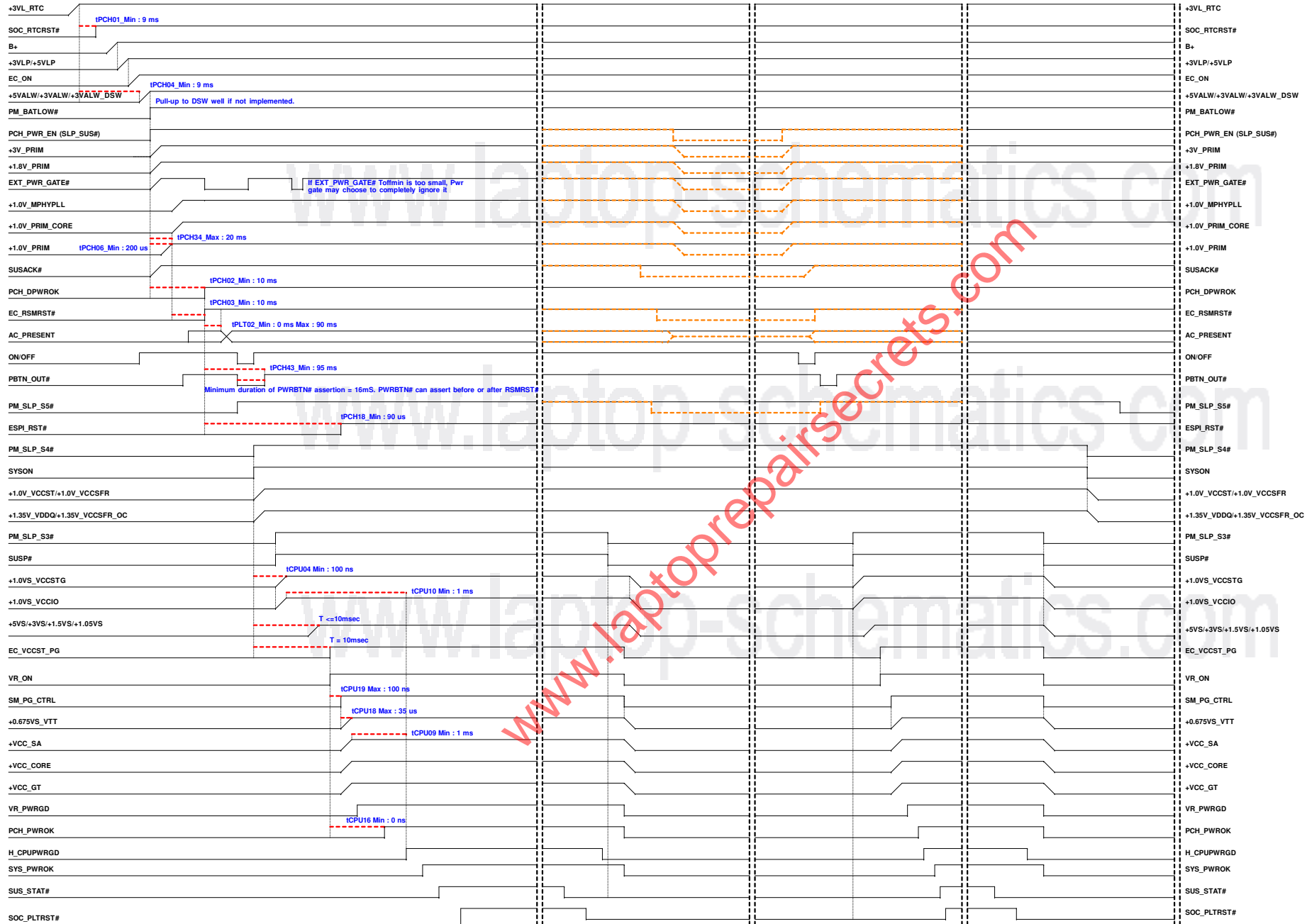


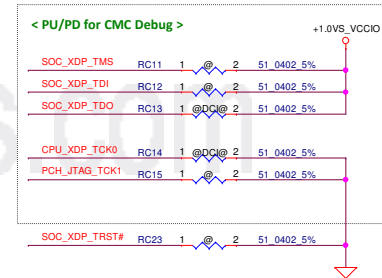
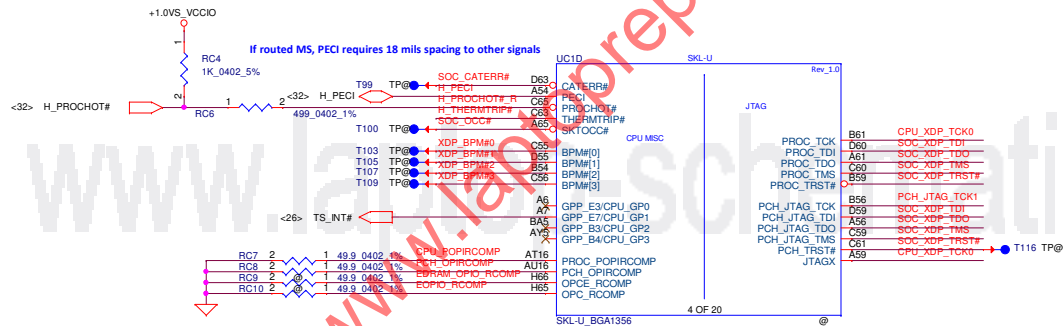
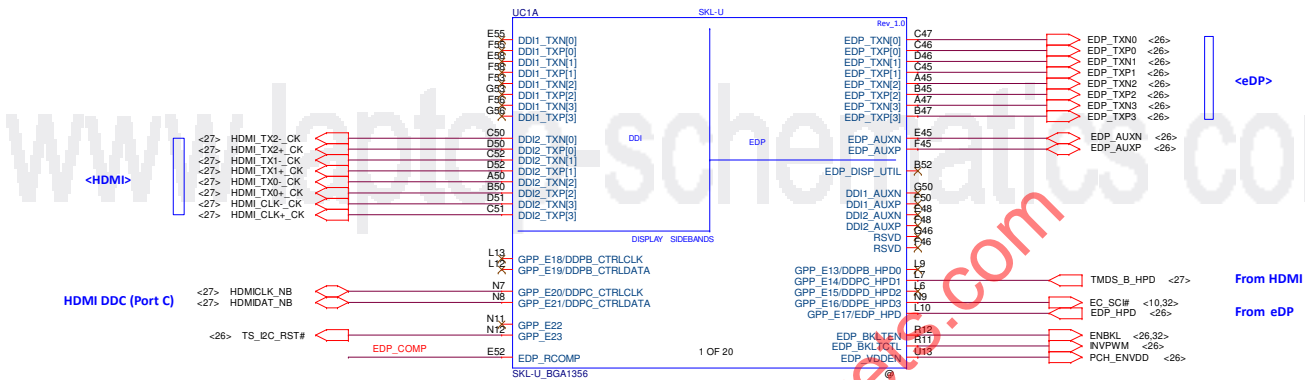
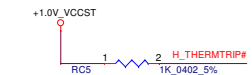
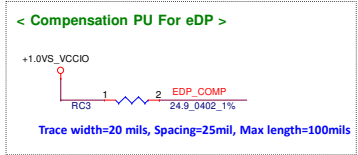
G3-&gt;S0

S0-&gt;S3/DS3

S0/DS3-&gt;S0

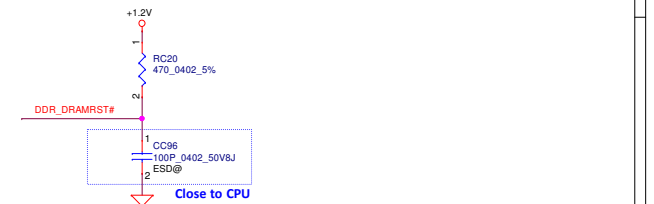
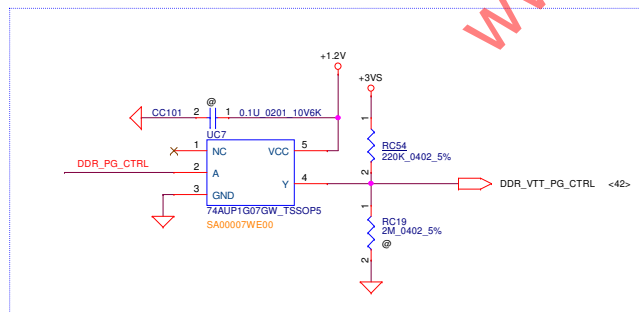
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				Document Number	2A
				Customer	LA-E541P
				Date	Wednesday, June 21, 2017
				Sheet	6 of 51

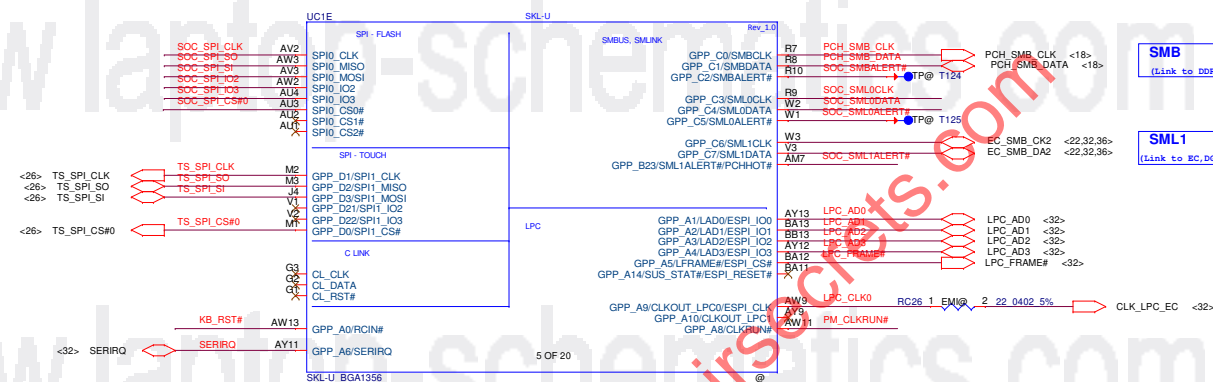
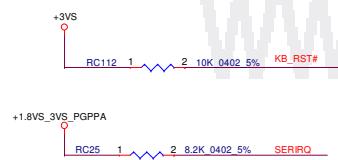
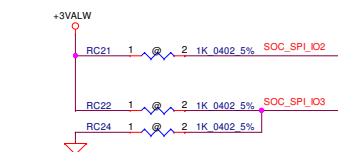
# Interleaved Memory



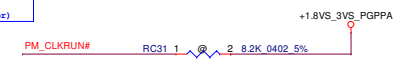
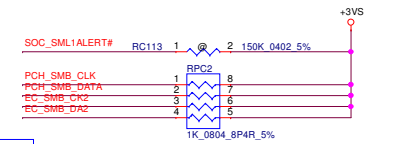
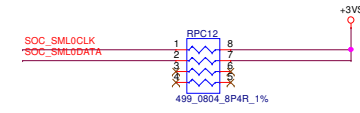
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Size	Document Number	LA-E541P	
Customer	LA-E541P	Rev 2A	

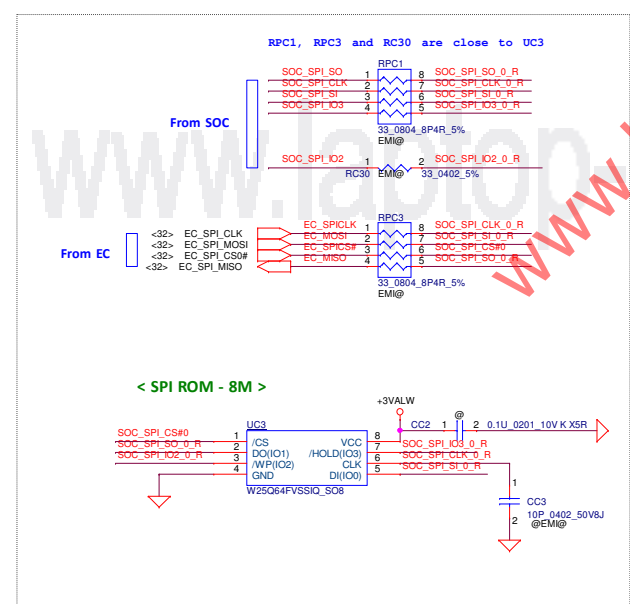




SML0ALERT# (Internal Pull Down):  
eSPI or LPC  
0 = LPC is selected for EC ==> Default  
1 = eSPI is selected for EC

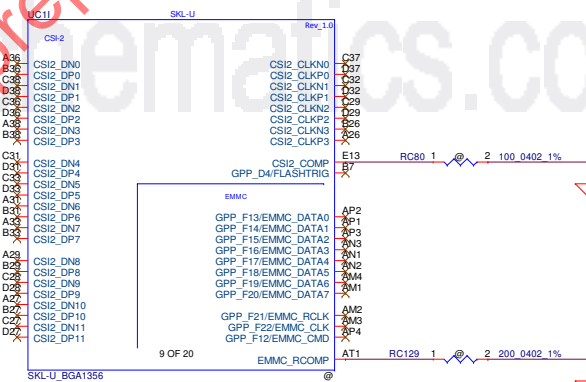
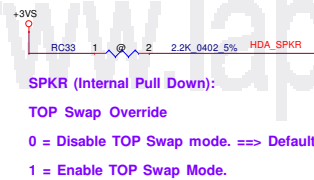
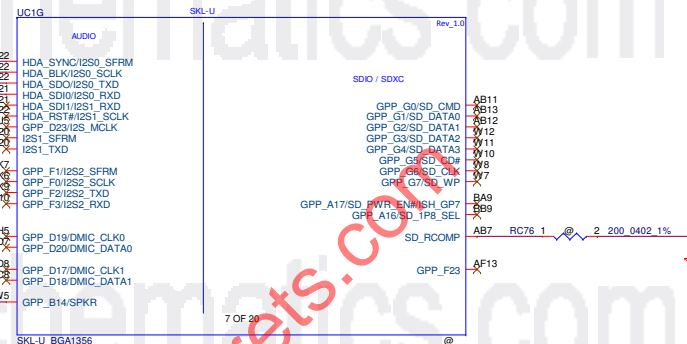
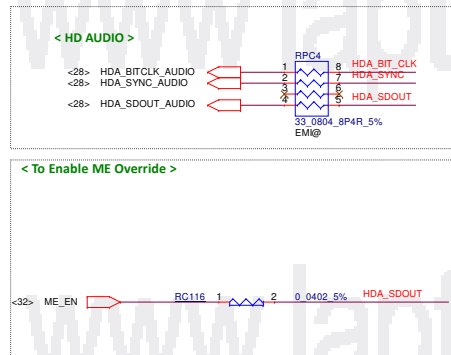


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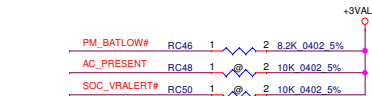
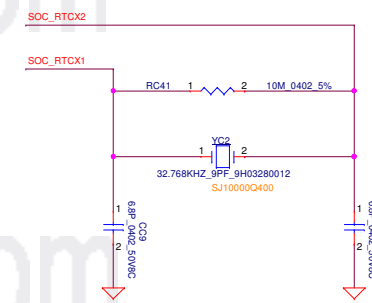
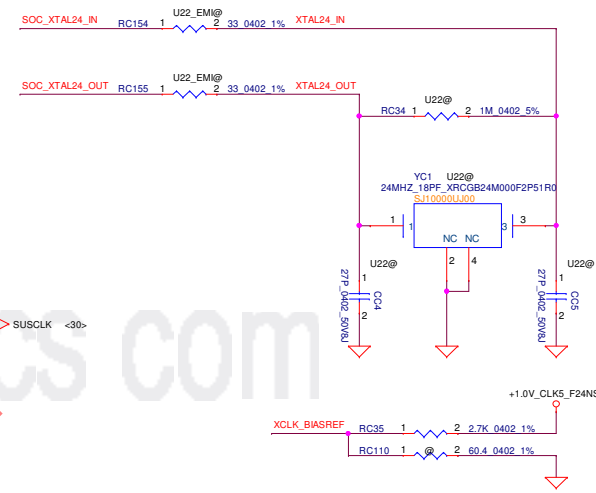
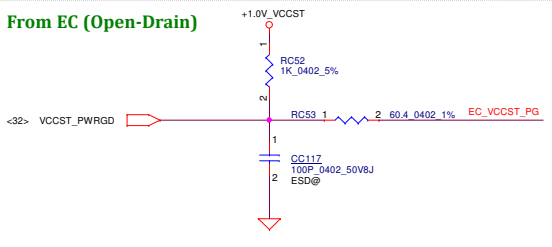
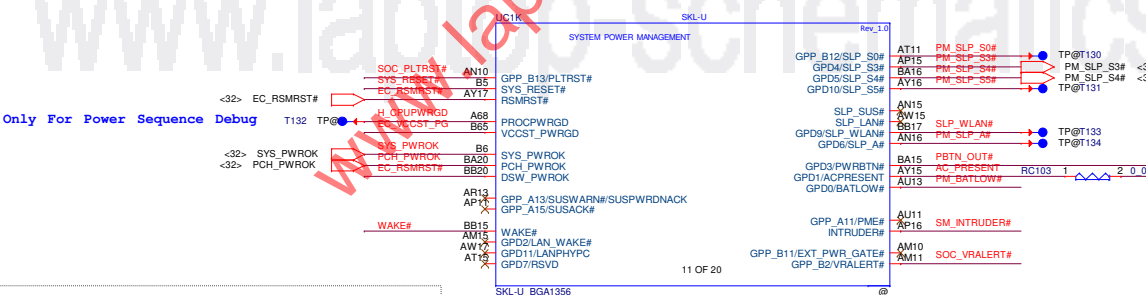
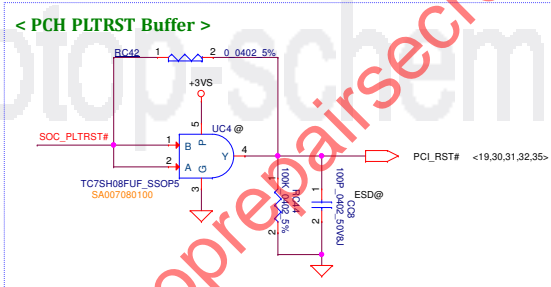
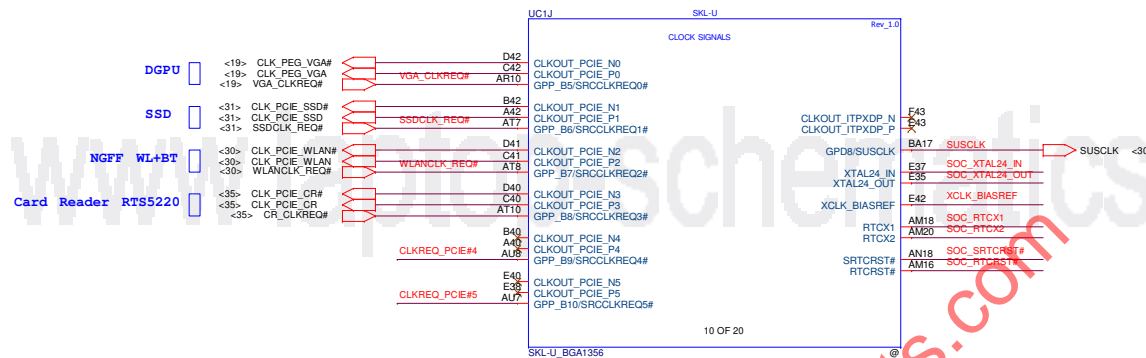
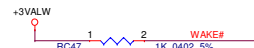
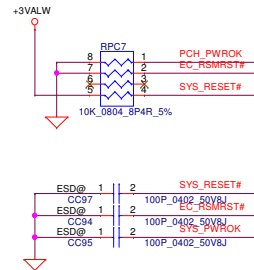
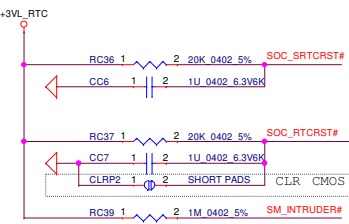
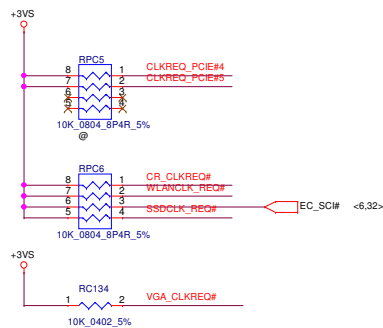


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				Size	Rev
				Custom	2A
				LA-E541P	
				Date:	Wednesday, June 21, 2017
				Sheet	8 of 51





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				Custom	LA-E541P
				Date:	Wednesday, June 21, 2017
				Sheet	9 of 51
				Rev	2A



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Issued Date	2017/06/05	Deciphered Date	2018/06/05			Title	SKL-U(5/12)CLK,PM,GPIO	
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						Date	Wednesday, June 21, 2017	Sheet 10 of 51

GPIO\_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

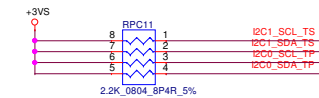
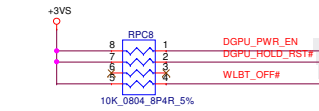
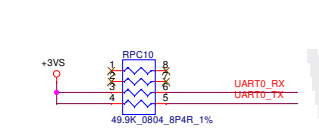
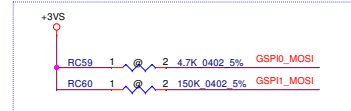
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Timer system reboot feature). This function is used  
when running ITP/XDP.

GPIO11\_MOSI (Internal Pull Down):

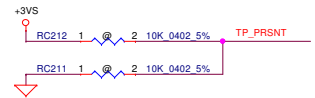
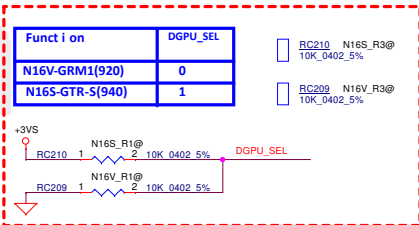
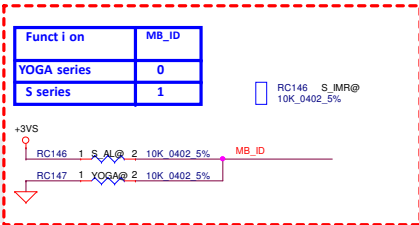
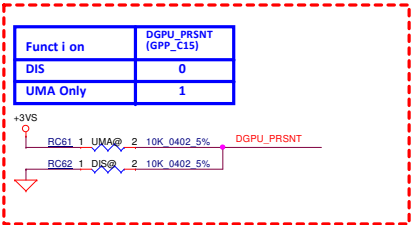
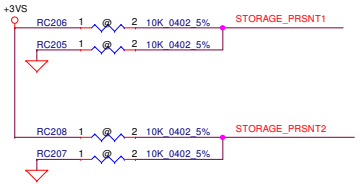
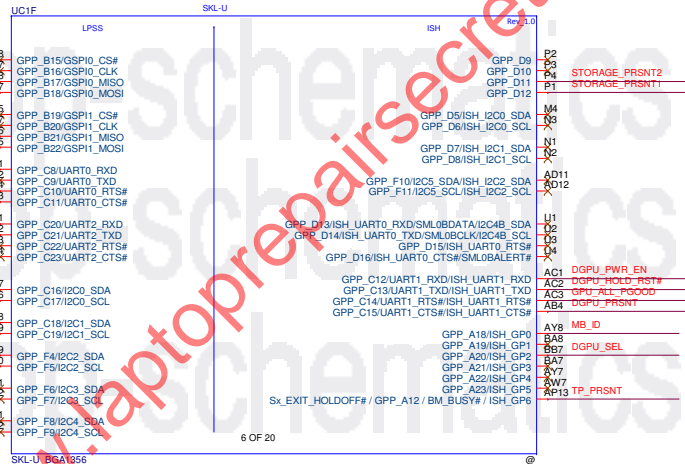
Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode



TO DGPU



dGPU

Card Reader

NGFF WLAN+BT

HDD

SSD

<19> PCIE\_PRX\_DTX\_N1  
<19> PCIE\_PRX\_DTX\_P1  
<19> PCIE\_PTX\_C\_DRX\_N1  
<19> PCIE\_PTX\_C\_DRX\_P1

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<19> PCIE\_PRX\_DTX\_P2  
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<19> PCIE\_PTX\_C\_DRX\_P4

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<30> PCIE\_PTX\_C\_DRX\_P6

<29> SATA\_PRX\_DTX\_N0  
<29> SATA\_PRX\_DTX\_P0  
<29> SATA\_PTX\_DRX\_N0  
<29> SATA\_PTX\_DRX\_P0

<31> PCIE\_PRX\_DTX\_N9  
<31> PCIE\_PRX\_DTX\_P9  
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<31> PCIE\_PTX\_C\_DRX\_P9

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<31> PCIE\_PRX\_DTX\_P10  
<31> PCIE\_PTX\_C\_DRX\_N10  
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<31> PCIE\_PTX\_C\_DRX\_P12

CC11 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N1  
CC14 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P1

CC15 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N2  
CC16 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P2

CC18 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N3  
CC13 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P3

CC17 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N4  
CC18 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P4

CC19 1 2 0.1U 0201 10V K XSR PCIE\_PTX\_DRX\_N5  
CC20 1 2 0.1U 0201 10V K XSR PCIE\_PTX\_DRX\_P5

CC102 1 2 0.1U 0201 10V K XSR PCIE\_PTX\_DRX\_N6  
CC103 1 2 0.1U 0201 10V K XSR PCIE\_PTX\_DRX\_P6

CC110 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N9  
CC109 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P9

CC114 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N10  
CC115 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P10

CC112 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N12  
CC111 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P12

RC71 1 2 100 0402 1% PCIE\_ROMPN  
PCIE\_ROMPN

T147 TP@# XDP\_PWDY#  
T148 TP@# XDP\_PWDY#

CC116 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N11  
CC115 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P11

CC112 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N12  
CC111 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P12

UC1H @ SKL-U

PCE / USB3 / SATA

H13 PCIE1\_RXN/USB3\_5\_RXN  
G13 PCIE1\_RXP/USB3\_5\_RXP  
B17 PCIE1\_TXN/USB3\_5\_TXN  
A17 PCIE1\_TXP/USB3\_5\_TXP

G11 PCIE2\_RXN/USB3\_6\_RXN  
F11 PCIE2\_RXP/USB3\_6\_RXP  
D16 PCIE2\_TXN/USB3\_6\_TXN  
C16 PCIE2\_TXP/USB3\_6\_TXP

H16 PCIE3\_RXN  
G16 PCIE3\_RXP  
D17 PCIE3\_TXN  
C17 PCIE3\_TXP

G15 PCIE4\_RXN  
F15 PCIE4\_RXP  
B19 PCIE4\_TXN  
A19 PCIE4\_TXP

F16 PCIE5\_RXN  
E16 PCIE5\_RXP  
C19 PCIE5\_TXN  
D19 PCIE5\_TXP

G18 PCIE6\_RXN  
F18 PCIE6\_RXP  
D20 PCIE6\_TXN  
C20 PCIE6\_TXP

F20 PCIE7\_RXN/SATA0\_RXN  
E20 PCIE7\_RXP/SATA0\_RXP  
B21 PCIE7\_TXN/SATA0\_TXN  
A21 PCIE7\_TXP/SATA0\_TXP

G21 PCIE8\_RXN/SATA1A\_RXN  
F21 PCIE8\_RXP/SATA1A\_RXP  
D21 PCIE8\_TXN/SATA1A\_TXN  
C21 PCIE8\_TXP/SATA1A\_TXP

E22 PCIE9\_RXN  
D22 PCIE9\_RXP  
B23 PCIE9\_TXN  
A23 PCIE9\_TXP

F25 PCIE10\_RXN  
E25 PCIE10\_RXP  
D23 PCIE10\_TXN  
C23 PCIE10\_TXP

F5 PCIE\_ROMPN  
E5 PCIE\_ROMPN

D56 PROC\_PWDY#  
D61 PROC\_PWDY#  
B11 GPP\_A7/PIRQA#

E28 PCIE11\_RXN/SATA1B\_RXN  
D24 PCIE11\_RXP/SATA1B\_RXP  
C24 PCIE11\_TXN/SATA1B\_TXN  
B25 PCIE11\_TXP/SATA1B\_TXP

F30 PCIE12\_RXN/SATA2\_RXN  
A25 PCIE12\_RXP/SATA2\_RXP  
B25 PCIE12\_TXN/SATA2\_TXN  
A25 PCIE12\_TXP/SATA2\_TXP

SKL-U BGAT356

SSC / USB3

H8 USB3\_1\_RXN  
G8 USB3\_1\_RXP  
C13 USB3\_1\_TXN  
D13 USB3\_1\_TXP

J6 USB3\_2\_RXN / SSC\_RXN  
H6 USB3\_2\_RXP / SSC\_RXP  
B13 USB3\_2\_TXN / SSC\_TXN  
A13 USB3\_2\_TXP / SSC\_TXP

H10 USB3\_3\_RXN  
B15 USB3\_3\_RXP  
D15 USB3\_3\_TXN  
A15 USB3\_3\_TXP

E10 USB3\_4\_RXN  
C10 USB3\_4\_RXP  
D15 USB3\_4\_TXN  
A15 USB3\_4\_TXP

AB9 USB20\_N1  
AB10 USB20\_P1

AD6 USB20\_N2  
AD7 USB20\_P2

AH2 USB20\_N3  
AH3 USB20\_P3

AD9 USB20\_N4  
AD10 USB20\_P4

AJ1 USB20\_N5  
AJ2 USB20\_P5

AF6 USB20\_N6  
AF7 USB20\_P6

AH1 USB20\_N7  
AH2 USB20\_P7

AF8 USB20\_N8  
AF9 USB20\_P8

AG1 USB20\_N9  
AG2 USB20\_P9

AH7 USB20\_N10  
AH8 USB20\_P10

AB6 USB2\_COMP  
G33 RC104 1 2 1K 0402 5%  
G4 RC105 1 2 1K 0402 5%

GPP\_E9/USB2\_OC0#  
GPP\_E10/USB2\_OC1#  
GPP\_E11/USB2\_OC2#  
GPP\_E12/USB2\_OC3#

GPP\_E4/DEVSLP0  
GPP\_E5/DEVSLP1  
GPP\_E6/DEVSLP2

GPP\_E0/SATAXP/PCIE0/SATA0P  
GPP\_E1/SATAXP/PCIE1/SATA0P1  
GPP\_E2/SATAXP/PCIE2/SATA0P2

GPP\_E8/SATALED#

8 OF 20

USB3\_RX1\_N &lt;34&gt;

USB3\_RX1\_P &lt;34&gt;

USB3\_TX1\_N &lt;34&gt;

USB3\_TX1\_P &lt;34&gt;

USB3\_RX2\_N &lt;35&gt;

USB3\_RX2\_P &lt;35&gt;

USB3\_TX2\_N &lt;35&gt;

USB3\_TX2\_P &lt;35&gt;

USB3\_RX3\_N &lt;35&gt;

USB3\_RX3\_P &lt;35&gt;

USB3\_TX3\_N &lt;35&gt;

USB3\_TX3\_P &lt;35&gt;

USB20\_N1 &lt;34&gt;

USB20\_P1 &lt;34&gt;

USB20\_N2 &lt;35&gt;

USB20\_P2 &lt;35&gt;

USB20\_N3 &lt;35&gt;

USB20\_P3 &lt;35&gt;

USB20\_N4 &lt;35&gt;

USB20\_P4 &lt;35&gt;

USB20\_N5 &lt;26&gt;

USB20\_P5 &lt;26&gt;

USB20\_N6 &lt;29&gt;

USB20\_P6 &lt;29&gt;

USB20\_N7 &lt;30&gt;

USB20\_P7 &lt;30&gt;

USB\_OC0# &lt;34&gt;

USB\_OC1# &lt;35&gt;

USB\_OC2# &lt;35&gt;

WL\_OFF# &lt;30&gt;

USB3 Type-C (MUX)

USB2/3 Port (MB)

USB2/3 Port (IO/B)

USB3 Type-C Port

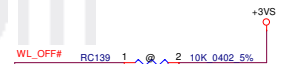
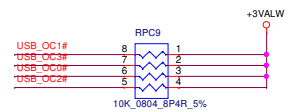
USB2/3 Port (MB)

USB2/3 Port (IO/B)

Camera

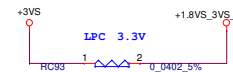
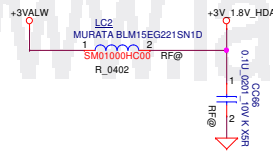
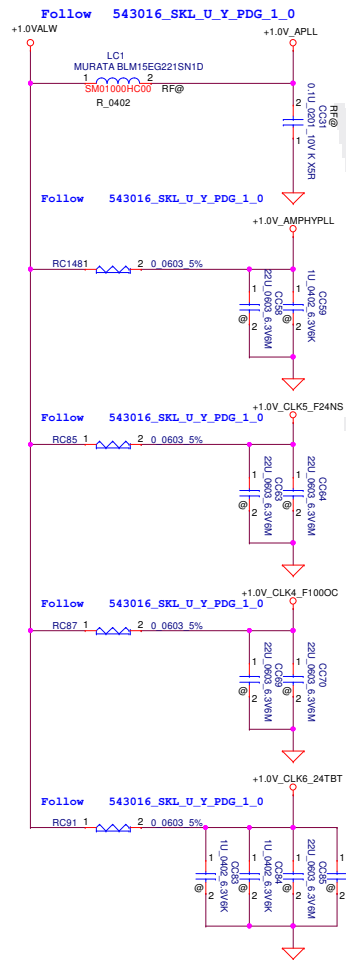
Finger Printer

NGFF WLAN+BT



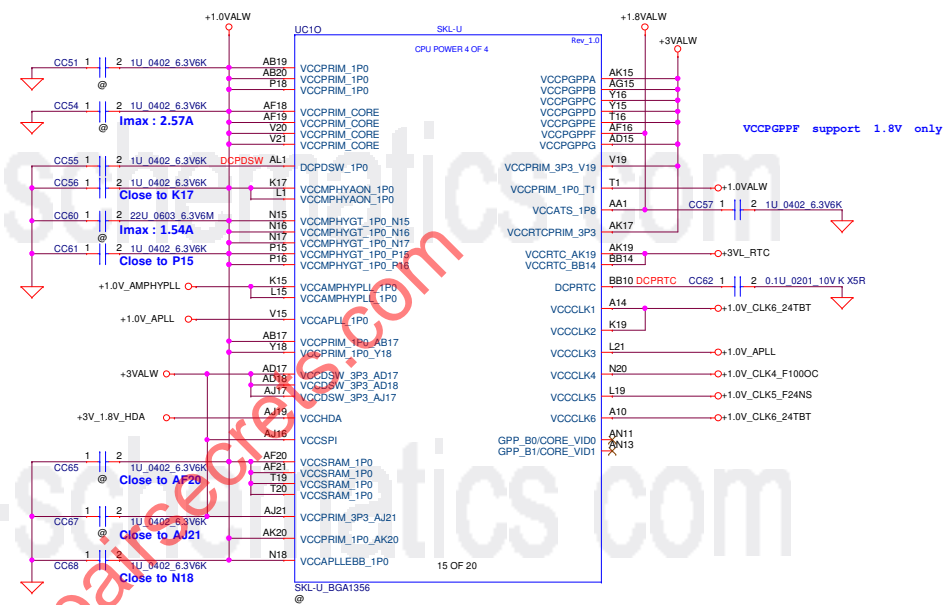
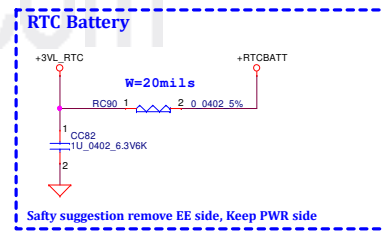
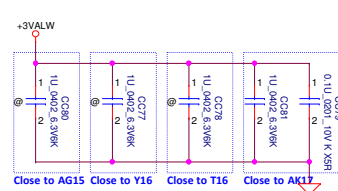
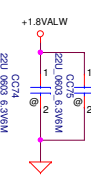
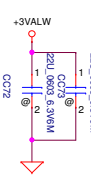
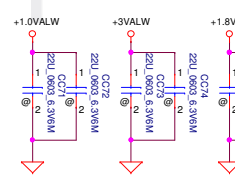
When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.





LPC 3.3V

+1.8V\_S\_VGPPA

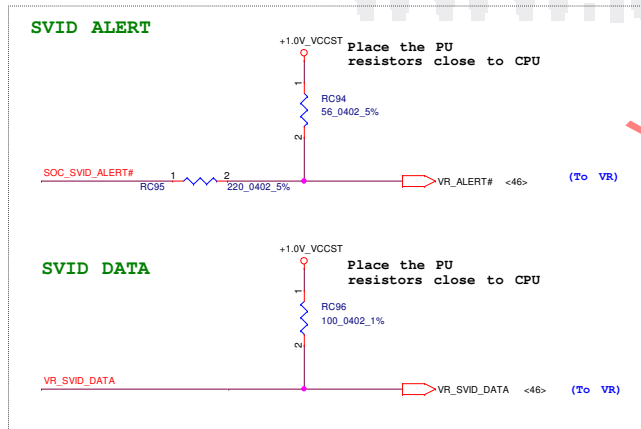
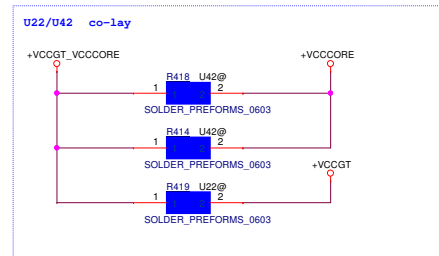
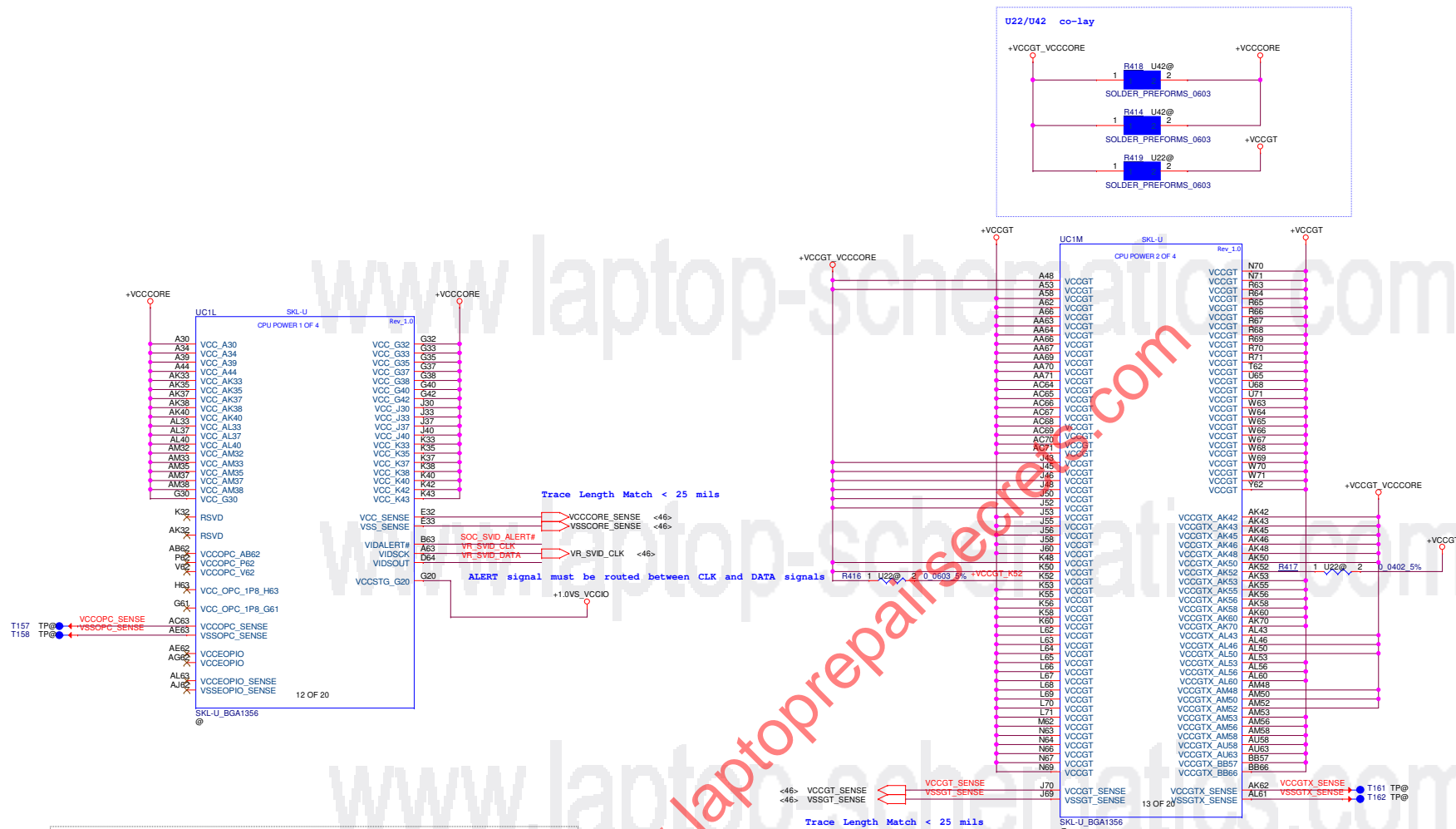


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				Sheet	14 of 51
				Rev	2A

Compal Electronics, Inc.

SKL-U(9/12)Power

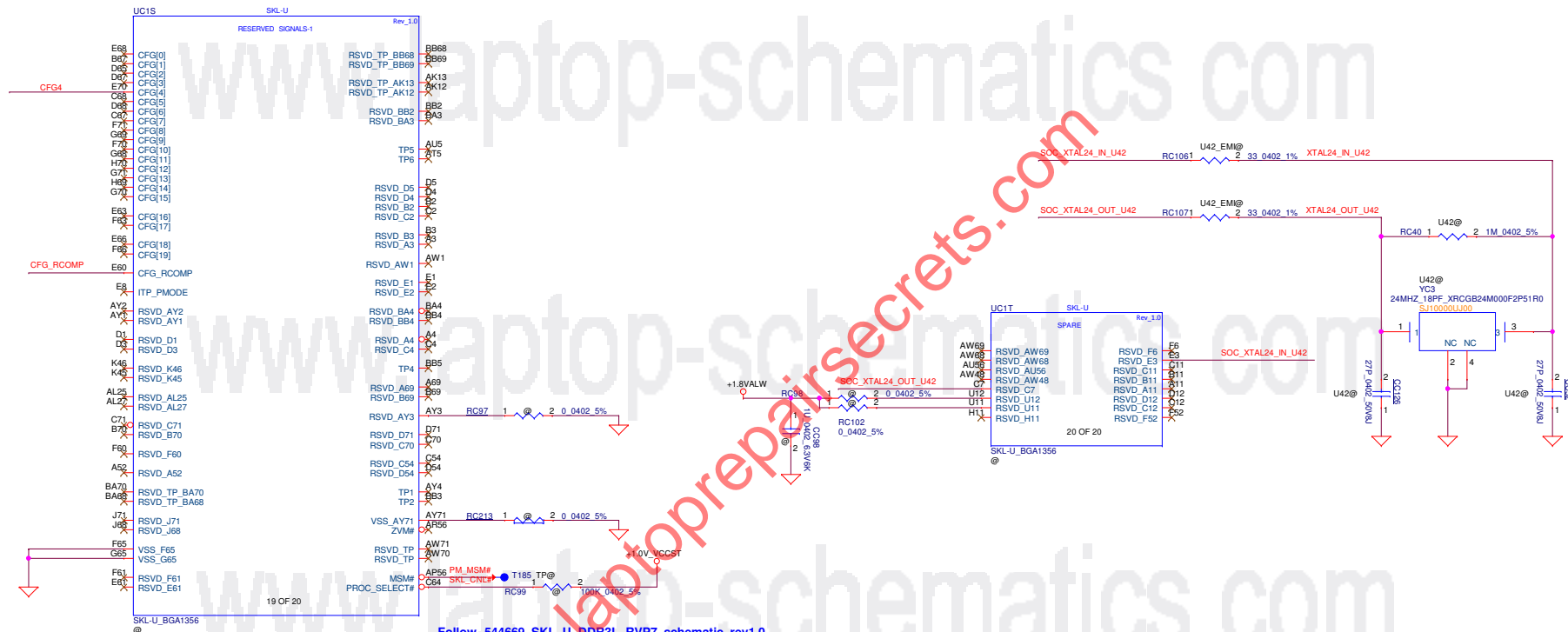
LA-E541P



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				Date:	Wednesday, June 21, 2017
				Sheet	15 of 51
				Rev	2A



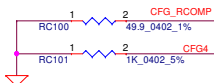




Follow 544669\_SKL\_U\_DDR3L\_RVP7\_schematic\_rev1.0

Stuff 100k(RC99) for CannonLake-U

Un-stuff 100k(RC99) for SkyLake-U



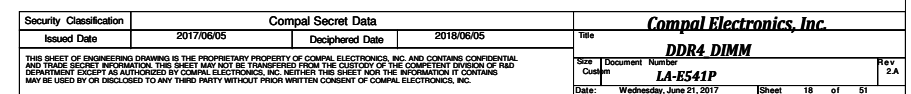
#### Display Port Presence Strap

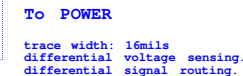
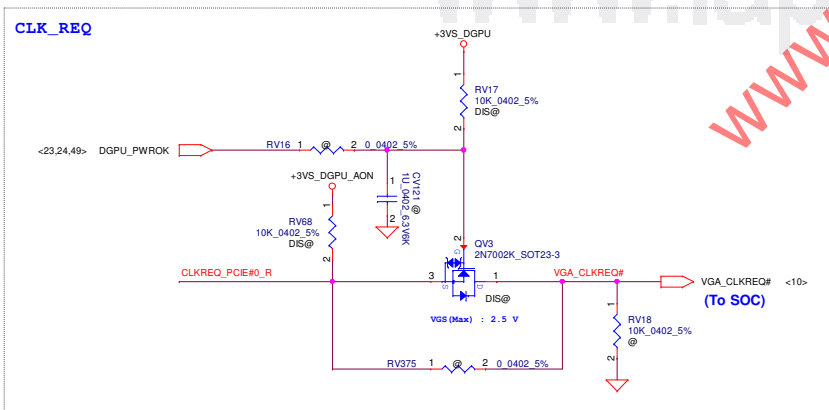
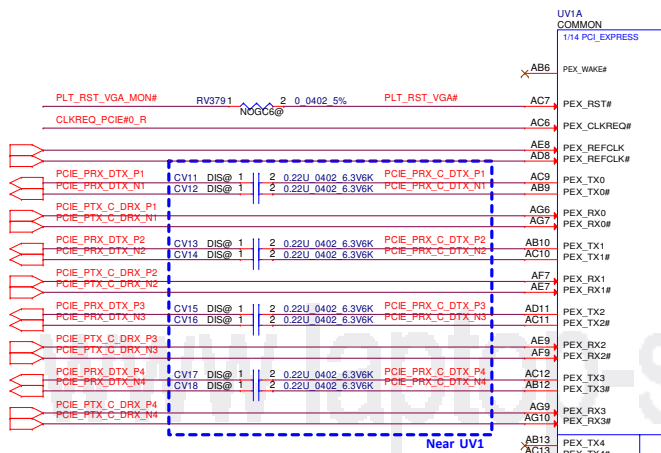
CFG4

1 : Disabled;  
No Physical Display Port attached to Embedded Display Port

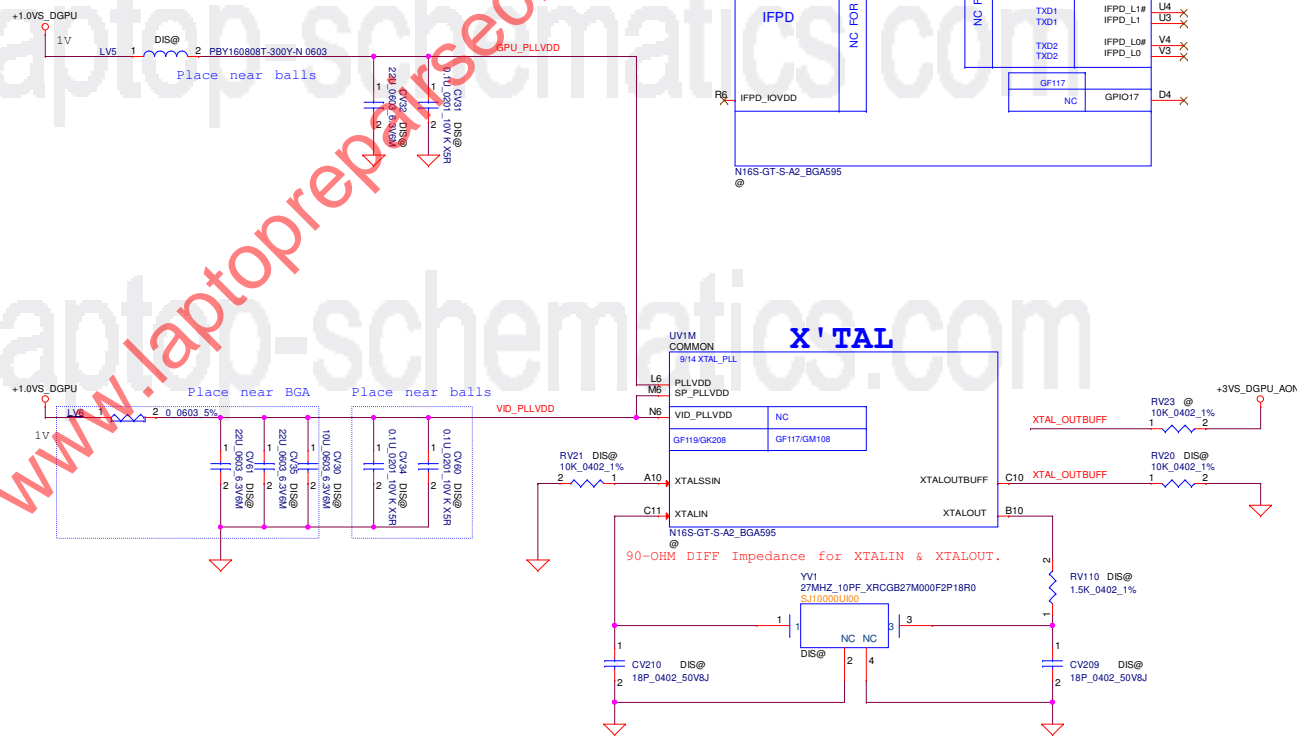
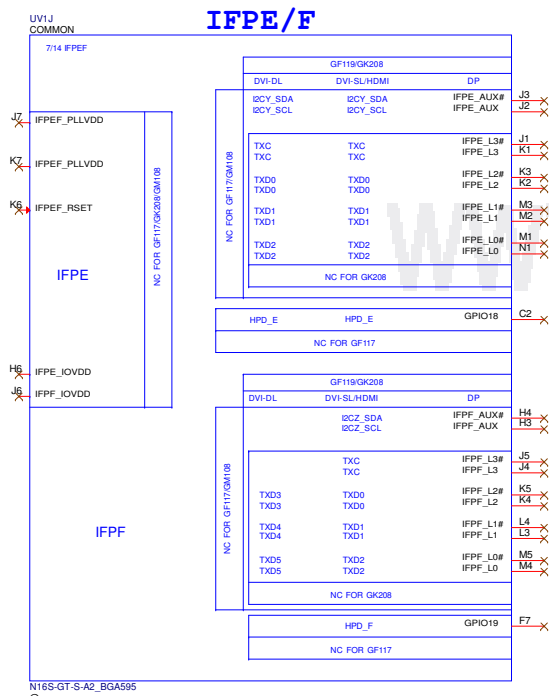
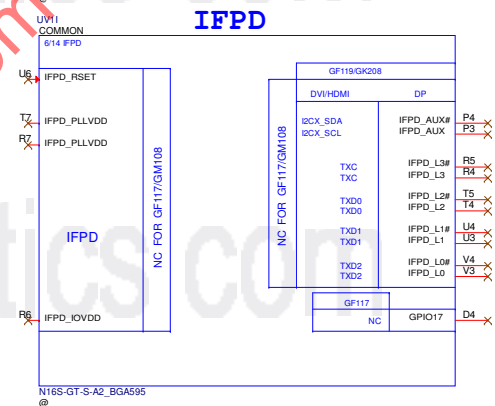
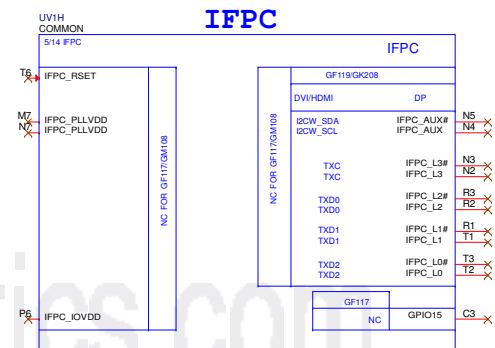
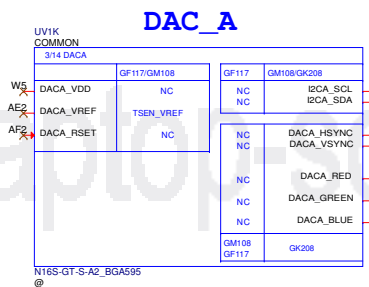
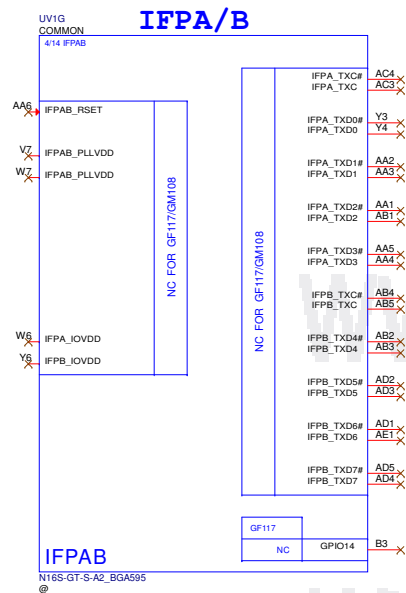
0 : Enabled;  
An external Display Port device is connected to the Embedded Display Port

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				Document Number	2A
				LA-E541P	
				Date:	Wednesday, June 21, 2017
				Sheet	17 of 51



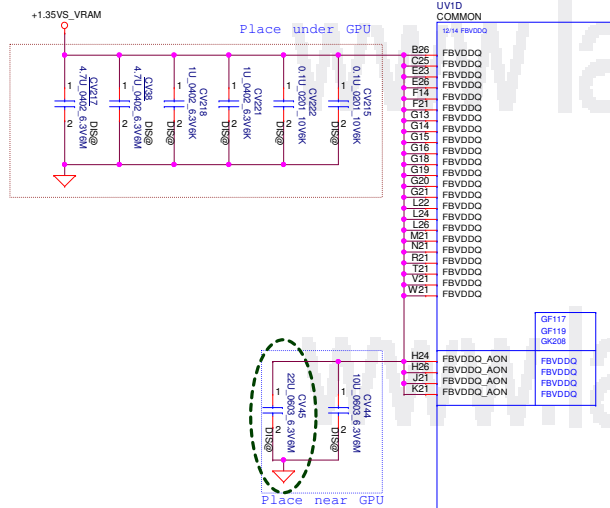


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					LA-E541P	2A
Date:				Wednesday, June 21, 2017	Sheet	19 of 51

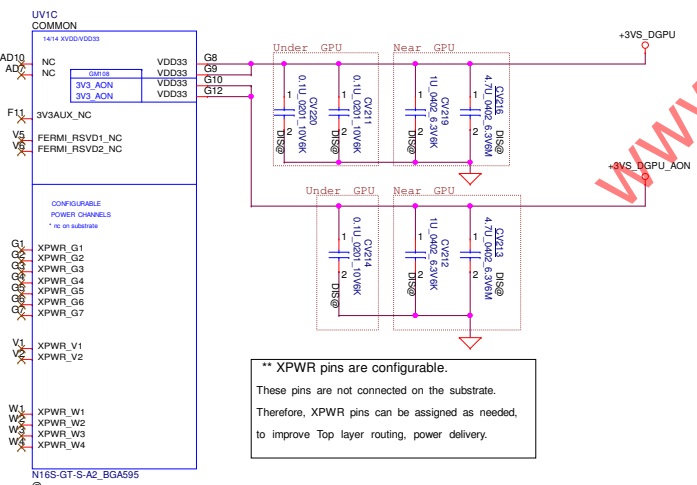
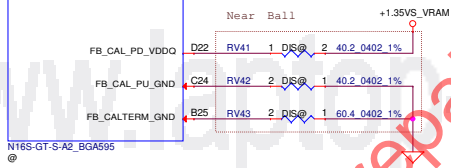


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Size		Document Number		Date		Wednesday, June 21, 2017		Sheet		20 of 51	
Rev		LA-E541P		Rev		2A					

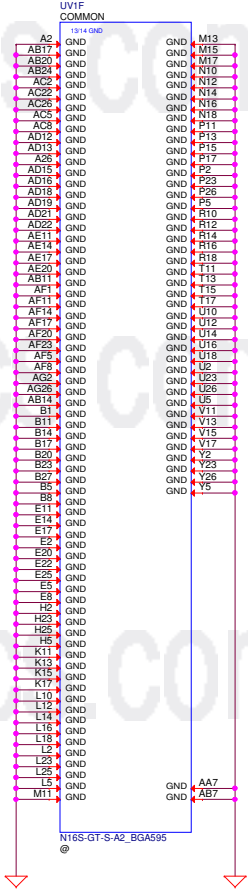
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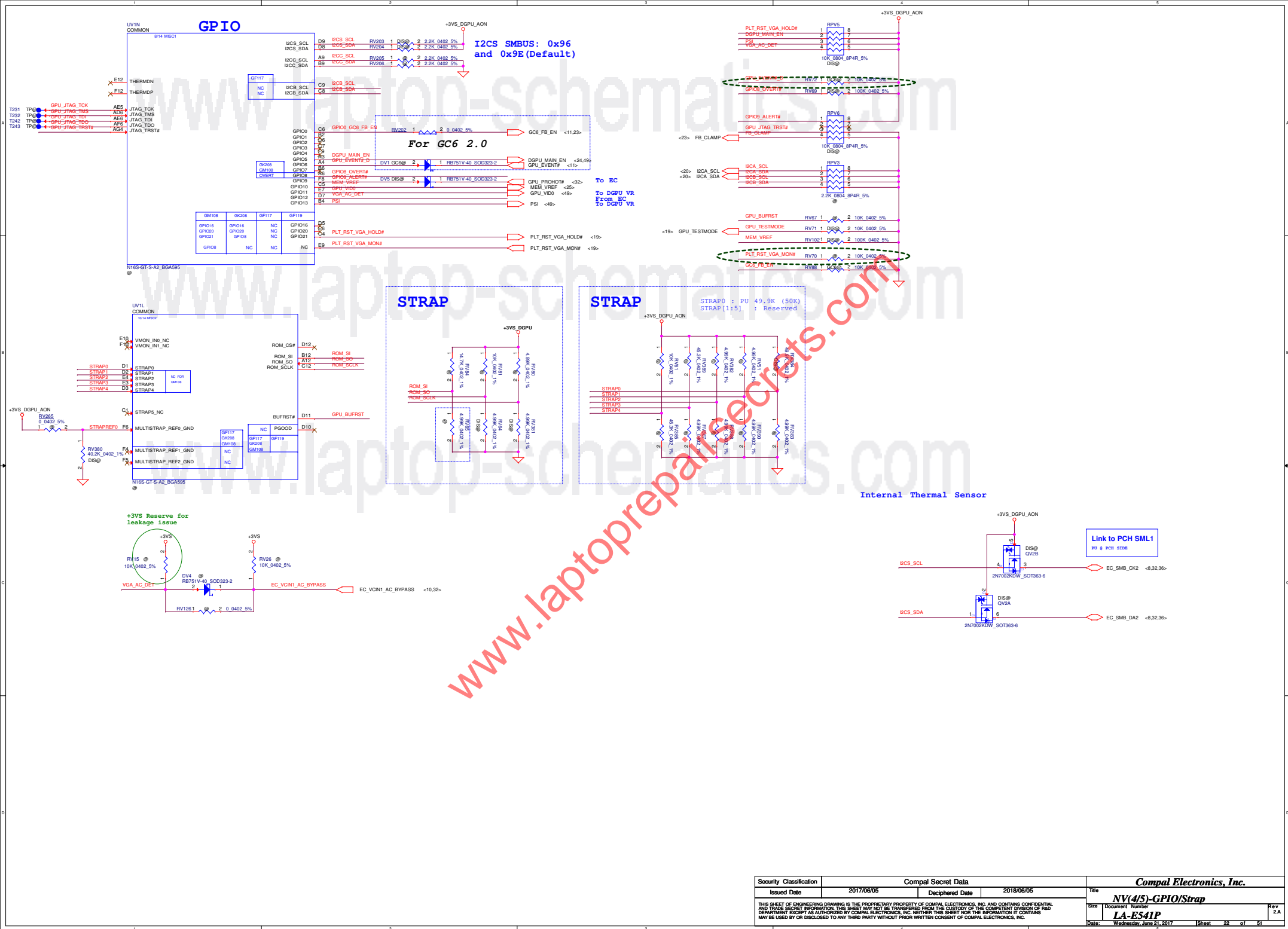
# GPU\_Decoupling CAPs @ Power Page



\*\* XPWR pins are configurable.  
These pins are not connected on the substrate.  
Therefore, XPWR pins can be assigned as needed,  
to improve Top layer routing, power delivery.



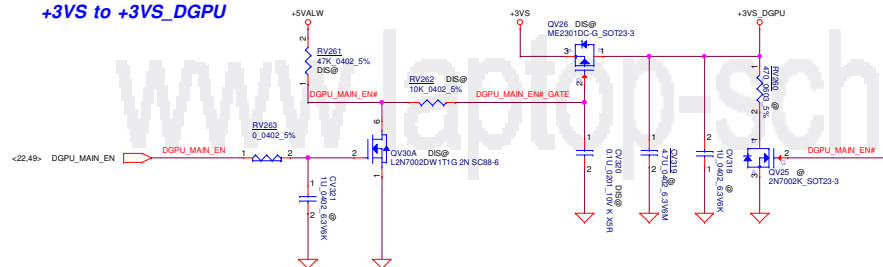
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				Sheet	21 of 51
				Rev	2A





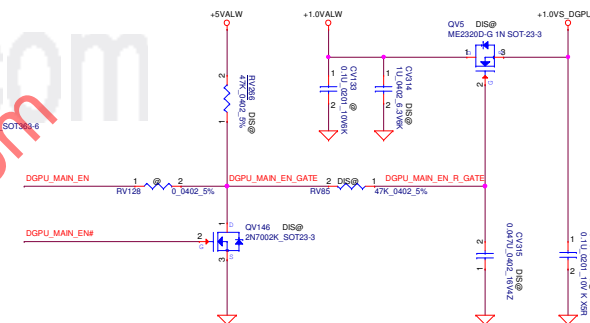


# +3VS to +3VS\_DGPU

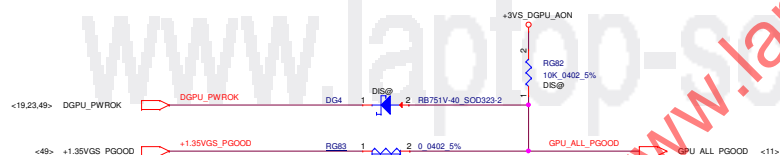
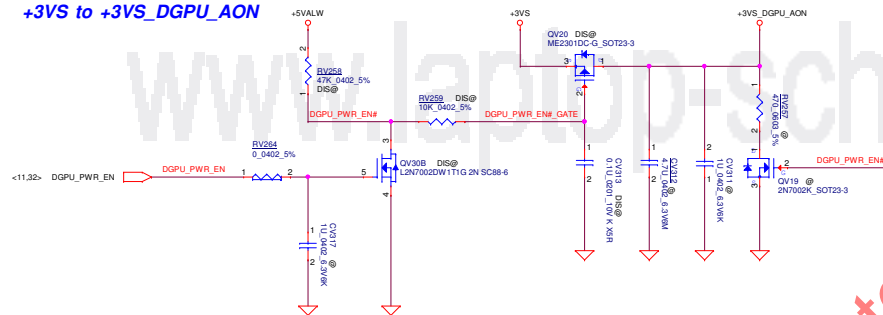


# +1.0V\_PRIM to +1.0VS\_DGPU

I Continuous (Max) : 0.79 A(+1.0VS\_DGPU)  
RON (Max) : 22 mohm  
V drop : 0.0175 V  
Rising : ~ 208us

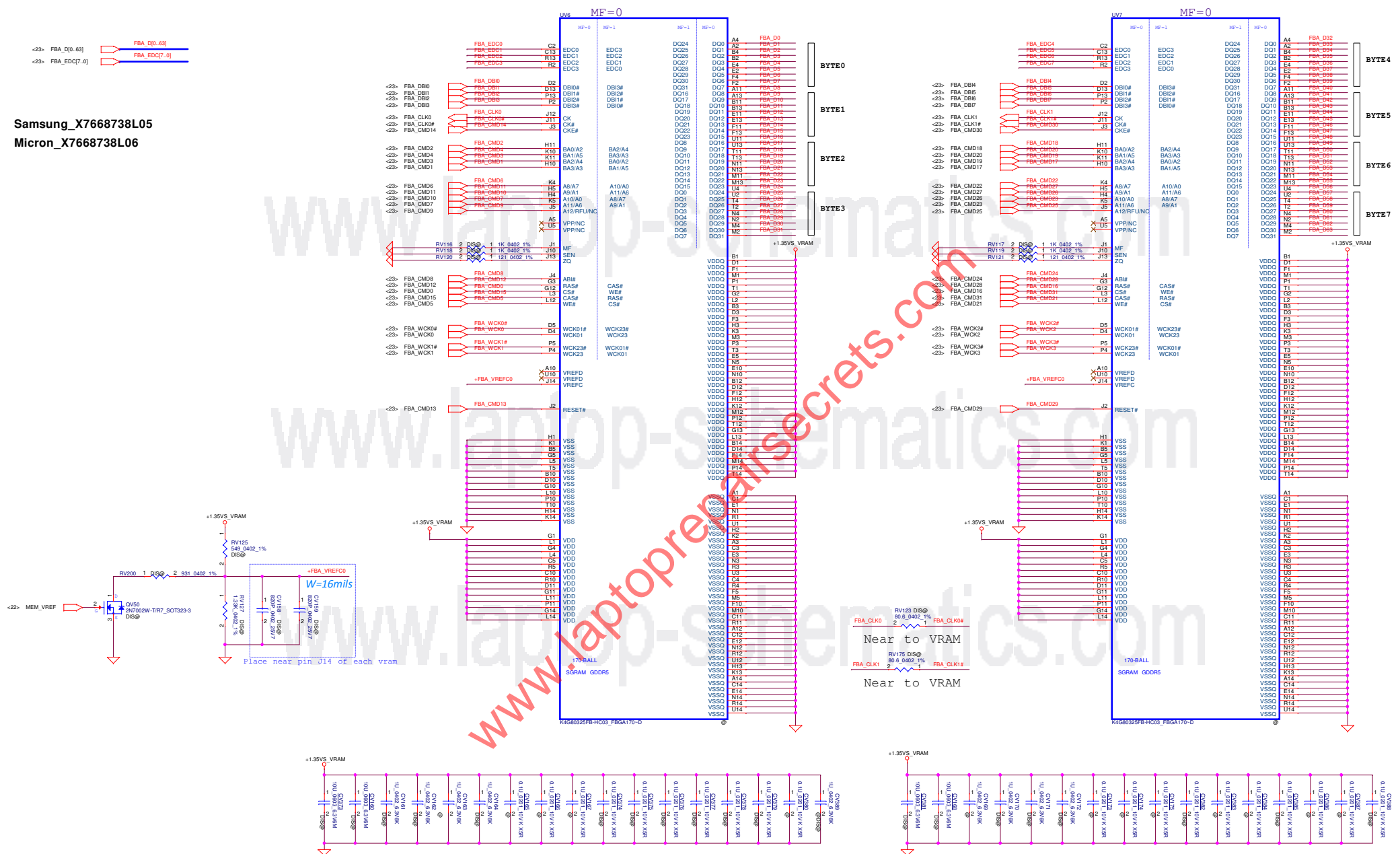


# +3VS to +3VS\_DGPU\_AON

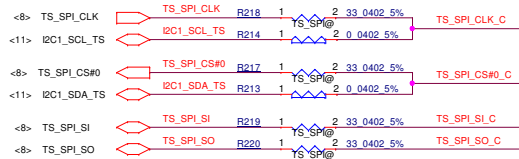
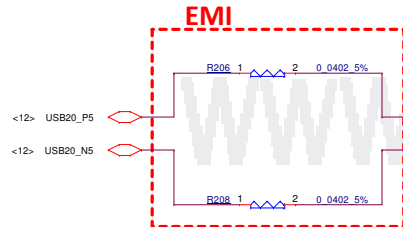
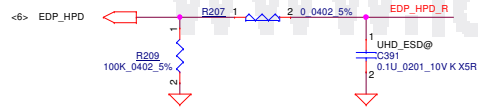
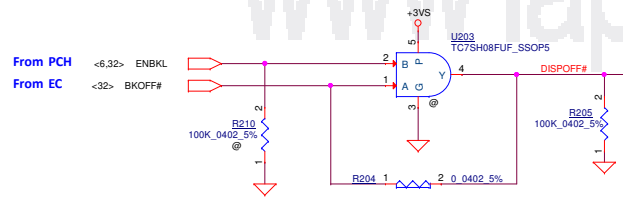
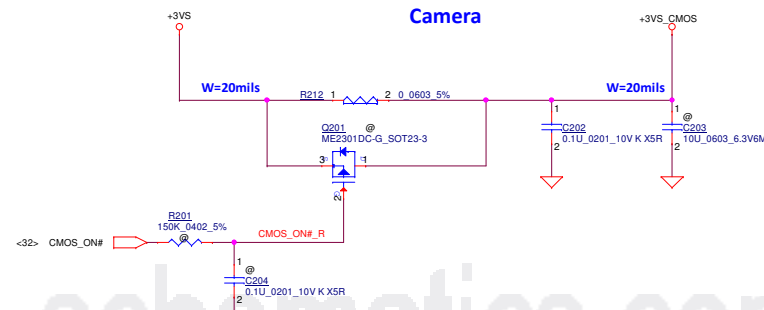
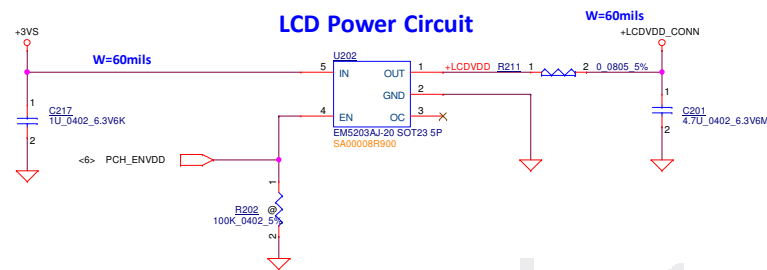


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Document Number				LA-E541P	
Date: Wednesday, June 21, 2017				Sheet 24	of 51

## Memory Partition A



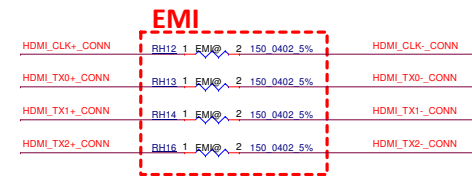
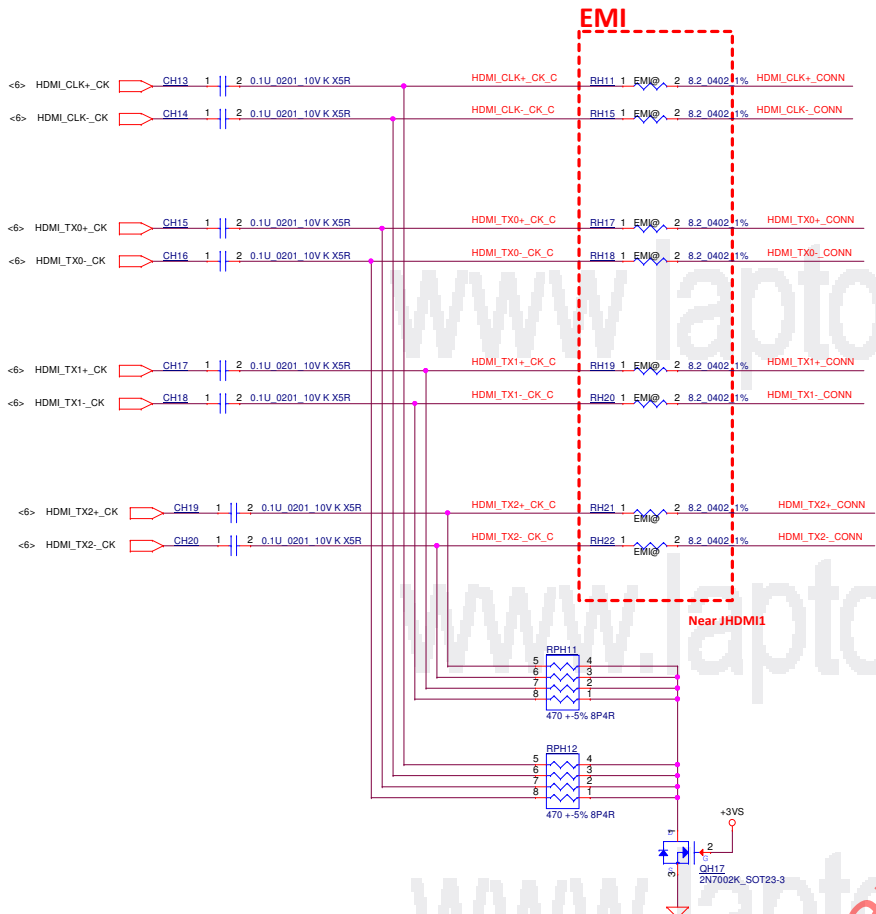
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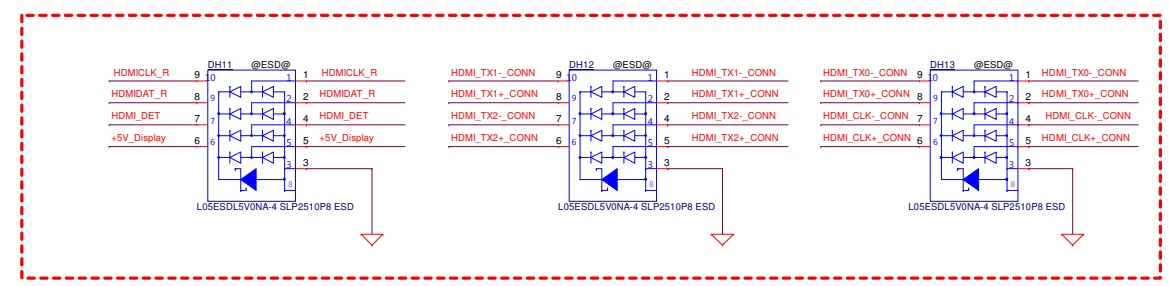
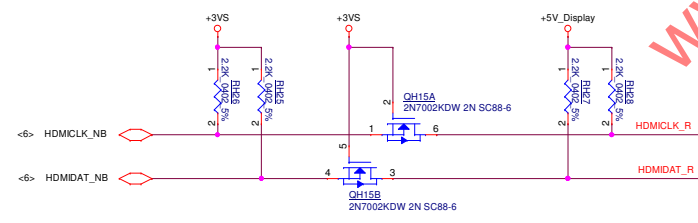
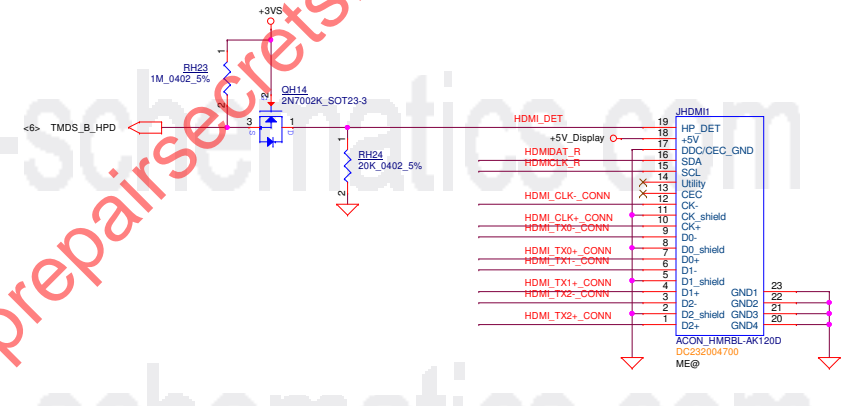
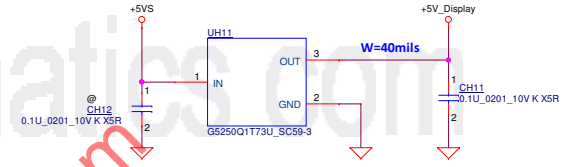
Elan Precise select by BOM (10 pins)		
1	PWR	PWR
2	CS	SCL
3	SCK	SDA
4	MOSI	Report switch
5	MISO	INT
6	Report switch	Reset
7	INT	Hsync
8	Reset	GND
9	Hsync	
10	GND	
Total	SPI (10 pins)	I2C (8 pins)

SPI & I2C PIN define	
1	PWR
2	SPI_Reset/I2C_Reset
3	Report_switch
4	GND
5	SPI_SCK/I2C_SCL
6	SPI_CS/I2C_SDA
7	SPI_MOSI
8	SPI_INT/I2C_INT
9	SPI_MISO
10	GND

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Size	Document Number	Date		Rev	
Custom	LA-E541P	Wednesday, June 21, 2017		2A	
Sheet		26		of 51	

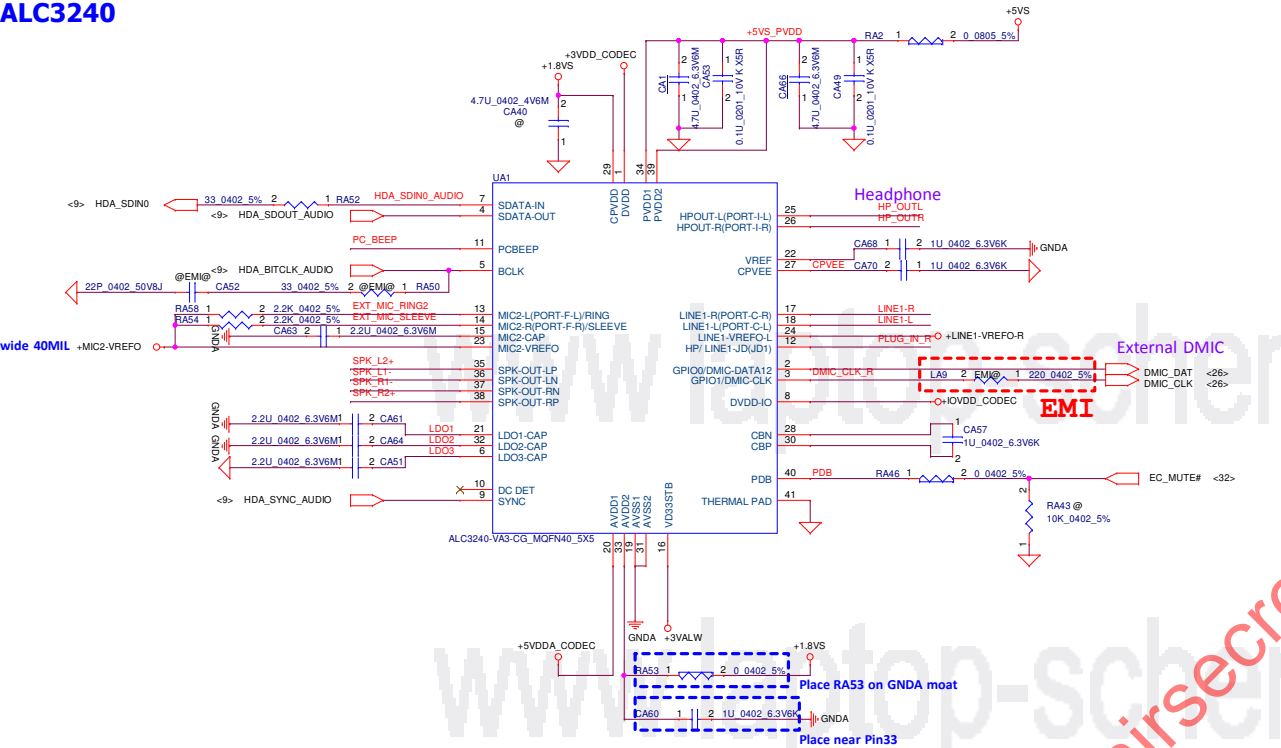


For HDMI

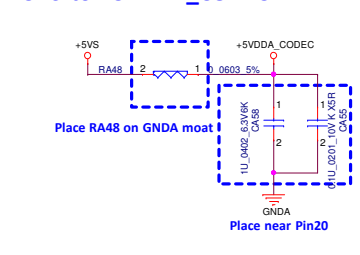


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				Size	Document Number
				Date: Wednesday, June 21, 2017	Rev 2A
				LA-E541P	Sheet 27 of 51

ALC3240



+5VS to +5VDDA\_CODEC



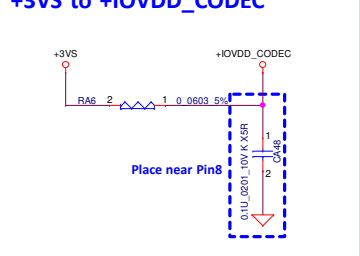
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
Intel Broadwell	1.5V (S0)	1.8V (S0)	3.3V (S0)	5V (S0)	3.3V (S0~S5)
Intel Skylake	V	V	V	V	V

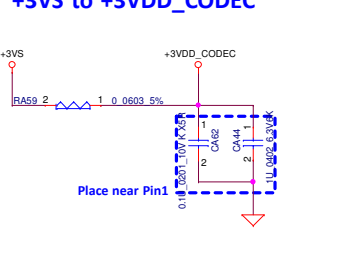
Each Platform HDA Link Voltage Support (Pin 8) :

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

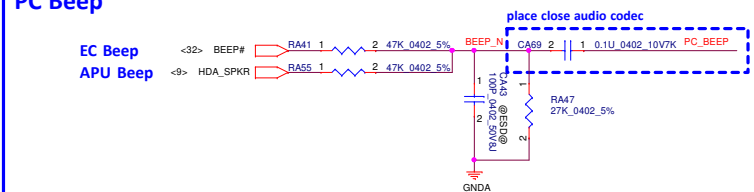
+3VS to +IOVDD\_CODEC



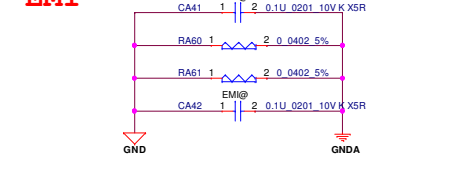
+3VS to +3VDD\_CODEC



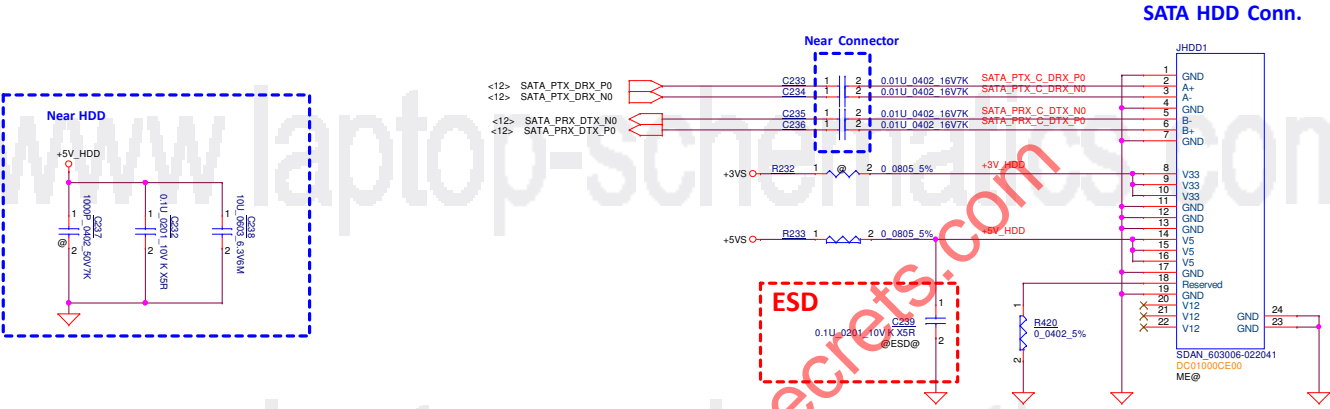
PC Beep



EMI

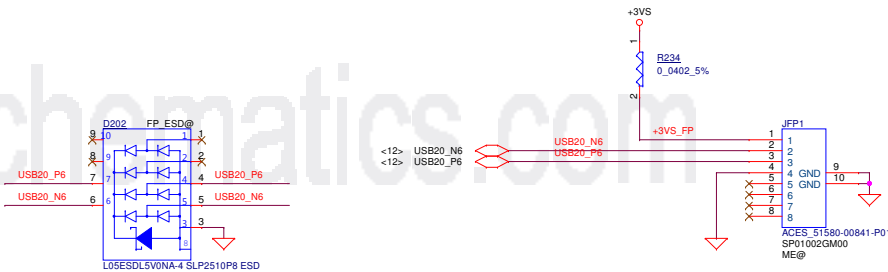
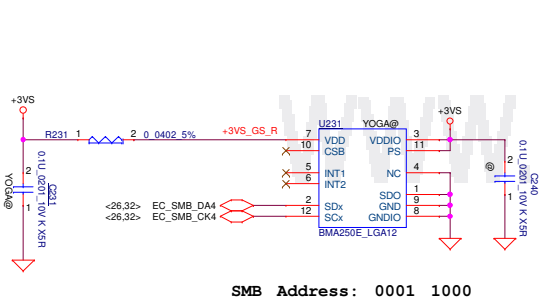


HDD



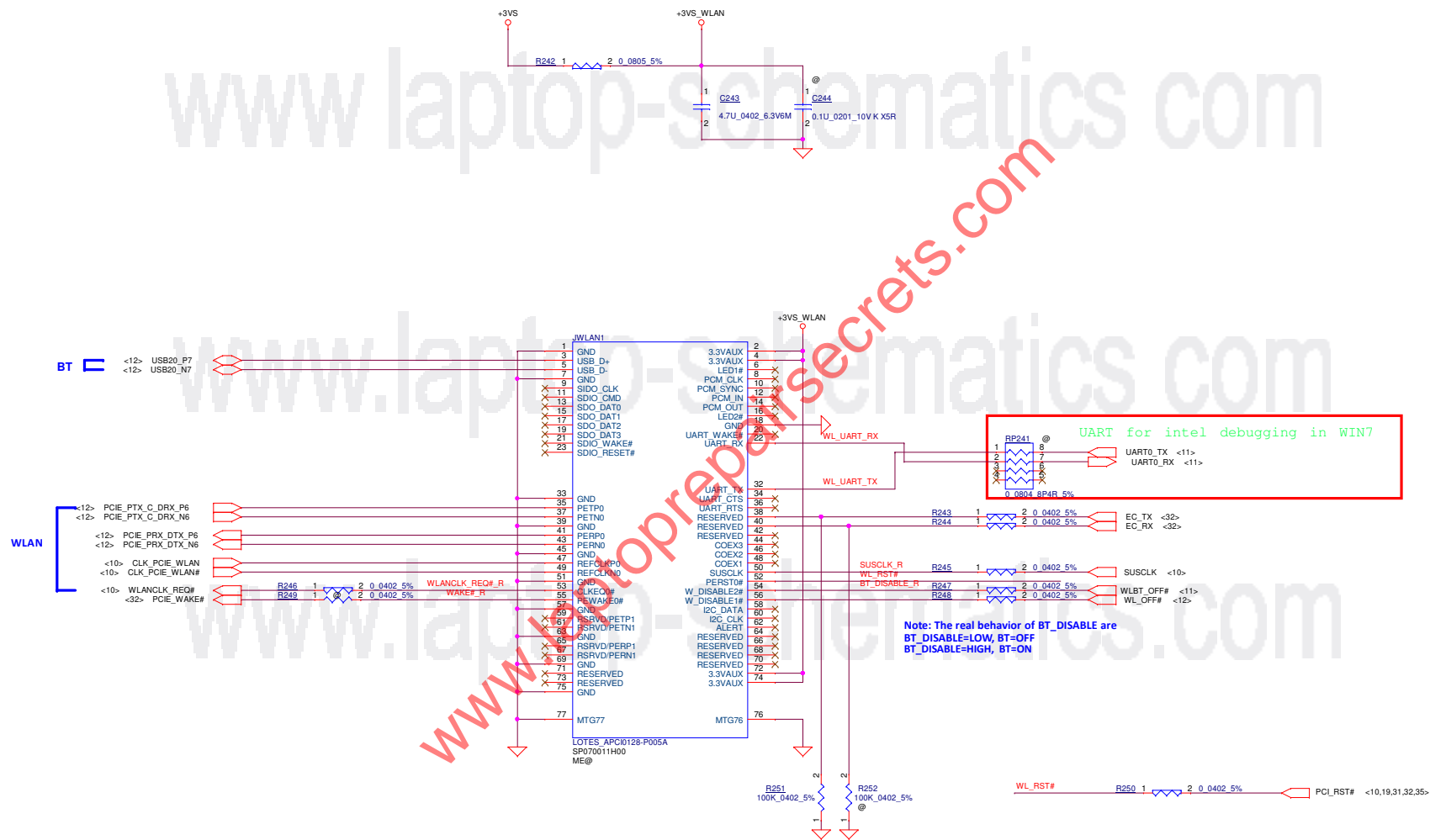
(G-Sensor for 360-degree reverse)

Finger Printer



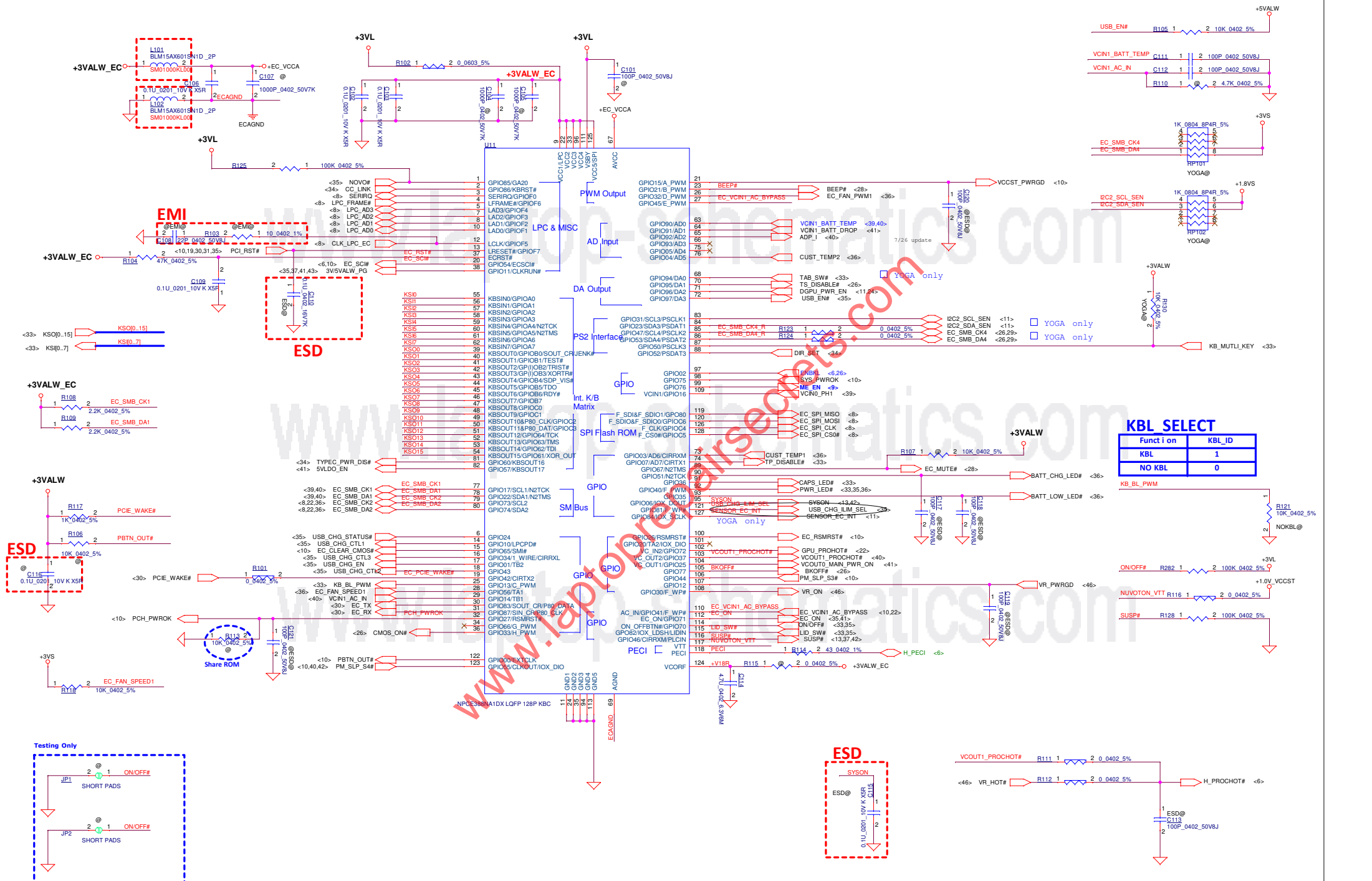


## NGFF for WLAN / BT (E- KEY)



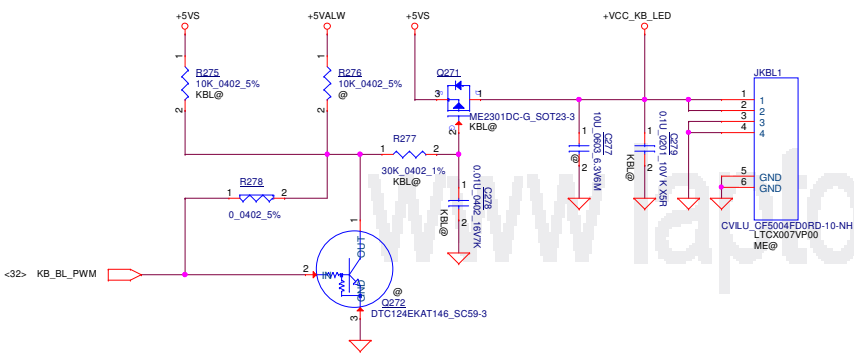
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				Size Document Number		Rev
				<b>LA-E541P</b>		<b>2A</b>
Date: Wednesday, June 21, 2017				Sheet	30	of 51

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				LA-E541P		2A
				Date: Wednesday, June 21, 2017	Sheet 31 of 51	

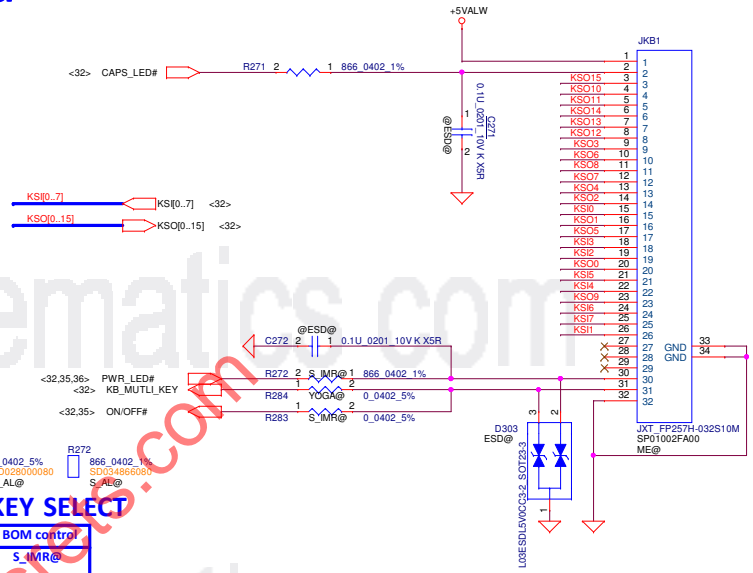


KBL SELECT	
Function	KBL_ID
KBL	1
NO KBL	0

Keyboard Backlight



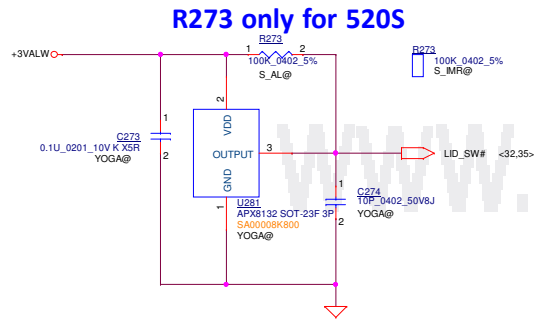
Keyboard



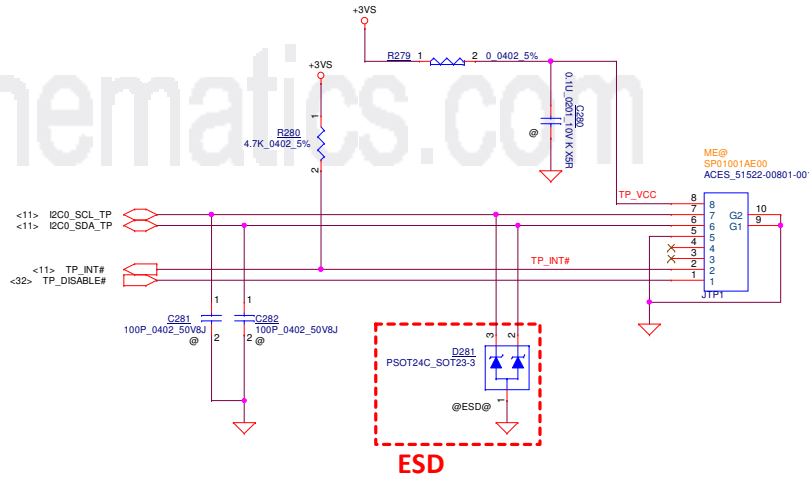
KB\_MUTLI\_KEY SELECT

Func1 on	BOM control
Power Key (Cruze )	S_1MR@
Func1 on Key (Alpine)	YOGA@

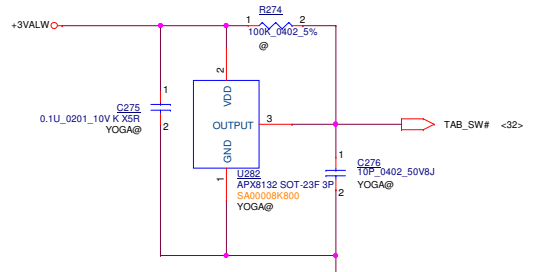
Hall -Sensor for 0-deg reverse (TOP)



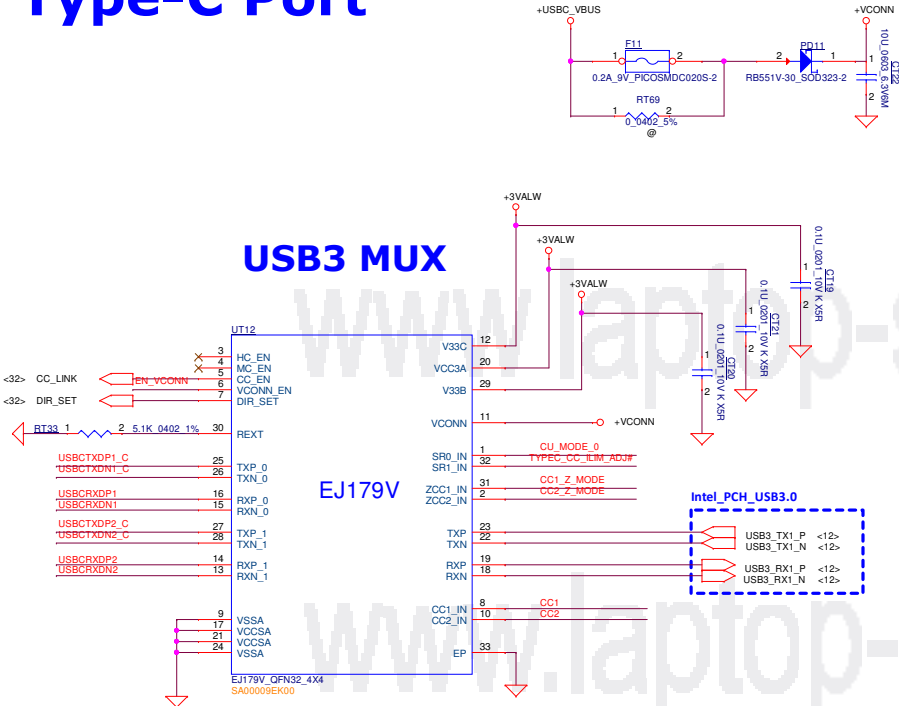
Touch Pad



Hall -Sensor for 360-deg reverse (BOT)



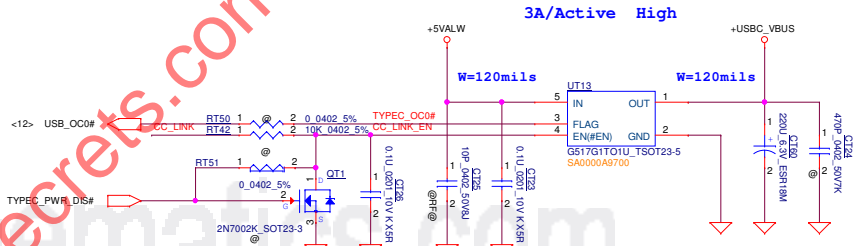
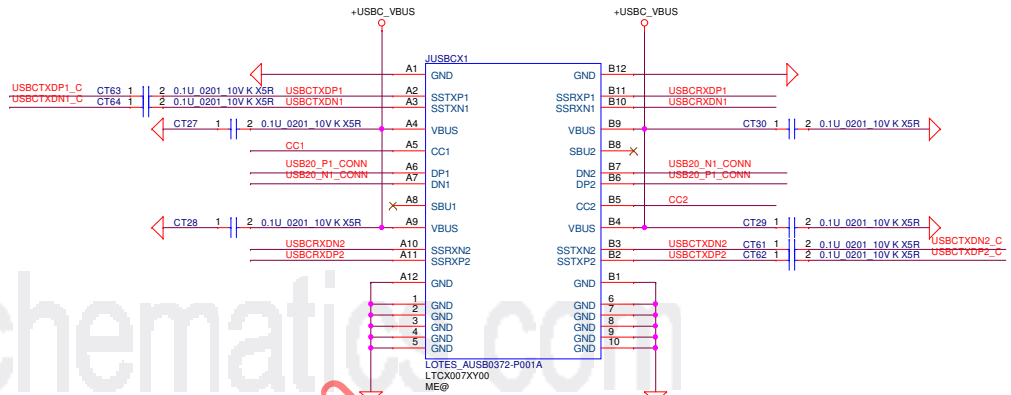
USB Type-C Port



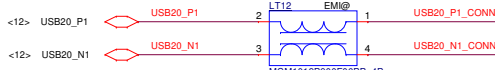
Profile Selection

EN_VCONN	CU_MODE_0	TYPECC_ILIM_ADJ#	CC[1:2]_Z_MODE	CURRNET SELECT
1	0	0	00	DFP 900mA
1	1	0	00	DFP 1.5A
1	0	1	00	DFP 3A
0	1	1	00	UFP
0	X	X	01 10 11	EXTERNAL RESISTER

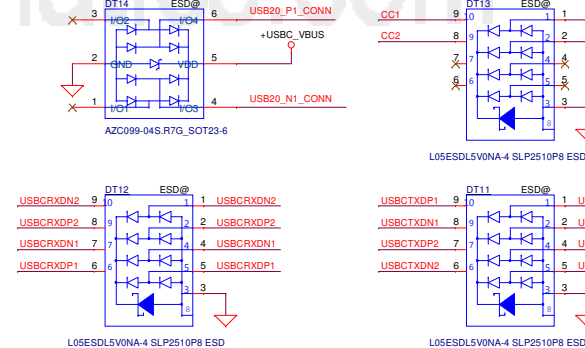
Currently setting



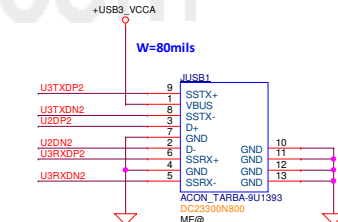
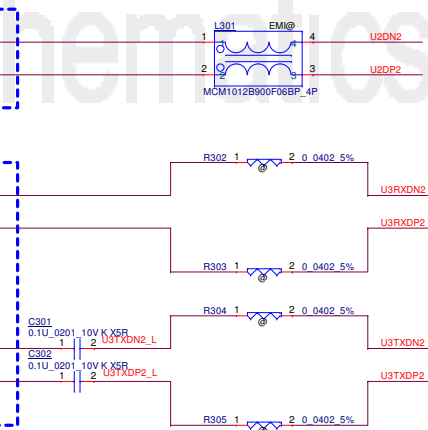
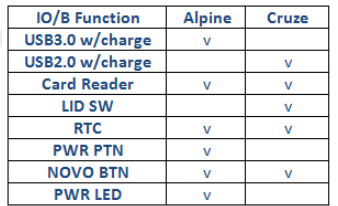
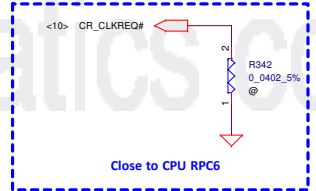
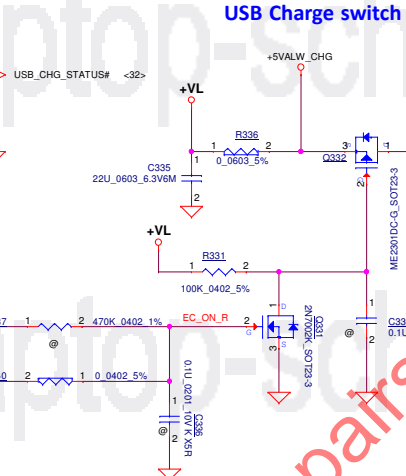
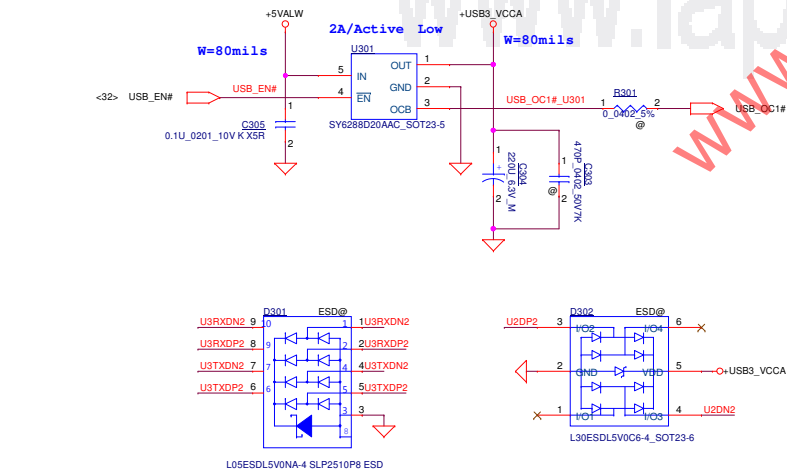
EMI



ESD



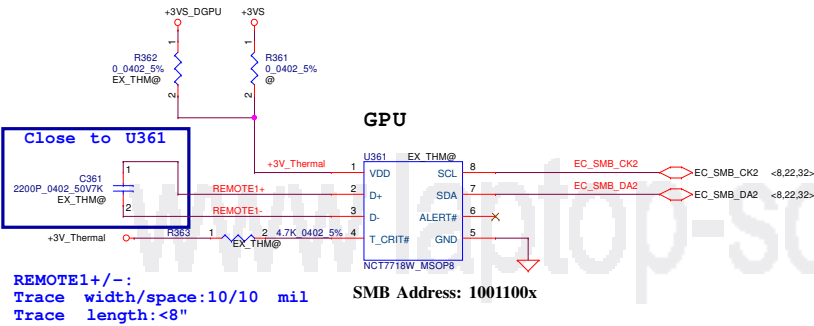
## USB3.0\_Port



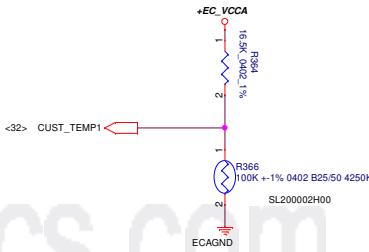
Place TX AC coupling Cap (C172,173). Close to connector

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				USB2 / USB3 / FP / IO Board		
				Size	Document Number	Rev
				Custom	LA-E541P	2A
				Date: Wednesday, June 21, 2017		Sheet 35 of 51

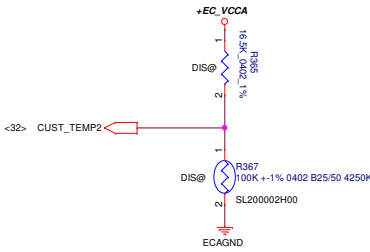
Thermal Sensor



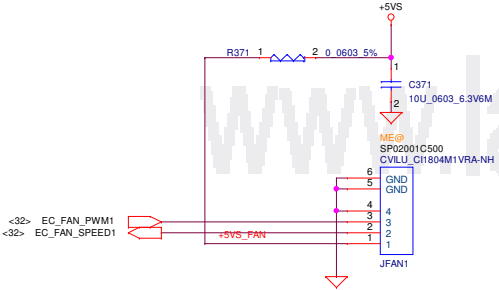
DDR



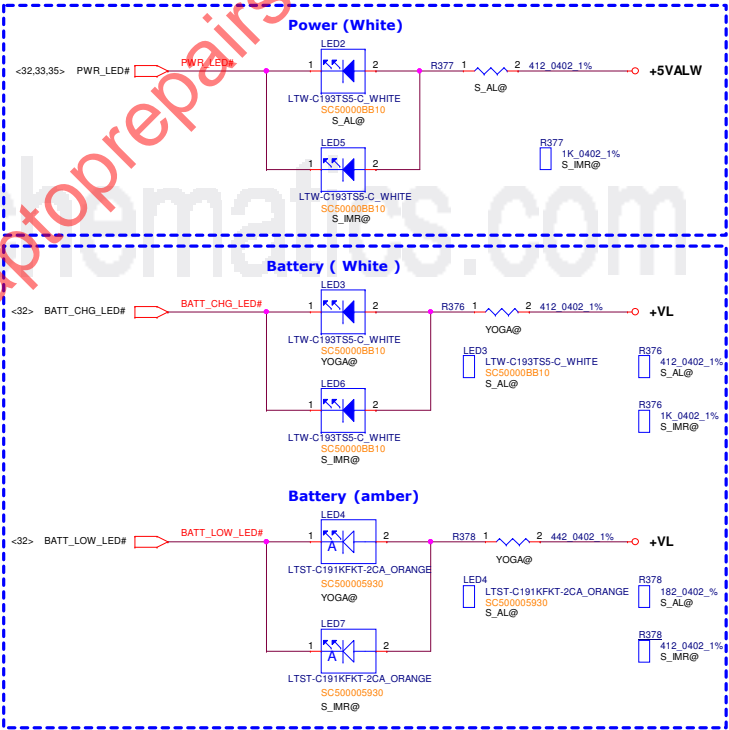
VRAM



FAN



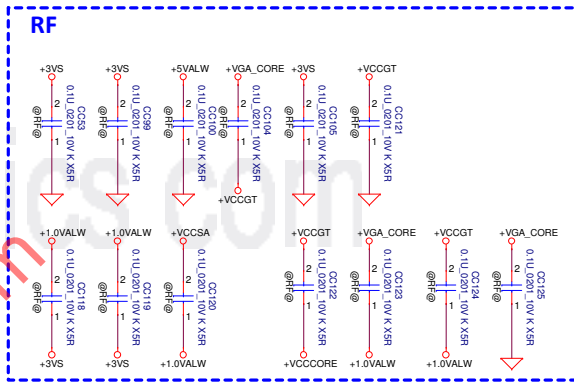
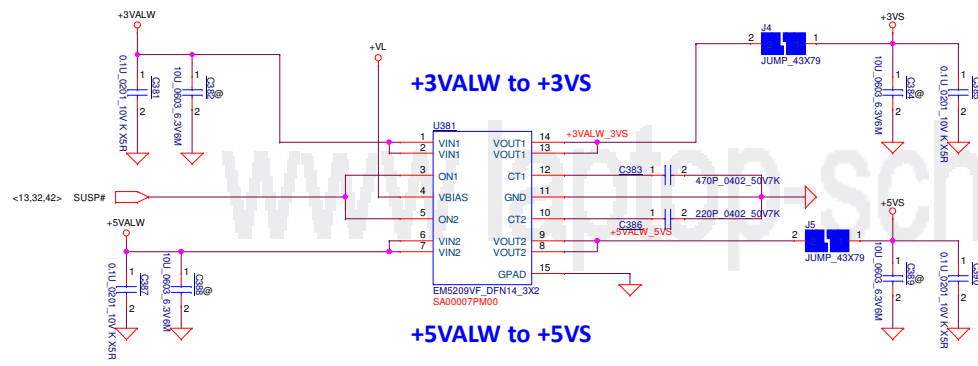
Power LED & Battery LED



		Power (White) LED / Res.	Battery (White) LED / Res.	Battery (amber) LED / Res.
TOP	YOGA (YOGA@)	IO Board	LED3	LED4
S series (S_AL@)	R377	412 Ω	LED3	LED4
S IMR (S_IMR@)	R377	1K Ω	LED6	LED7

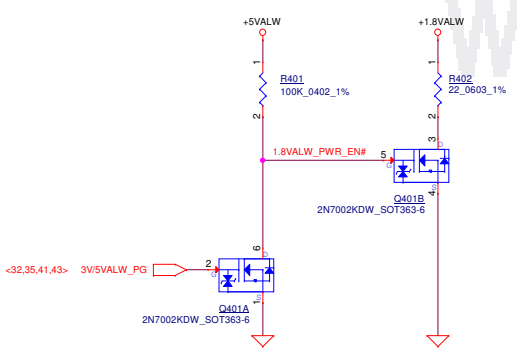


DC to DC

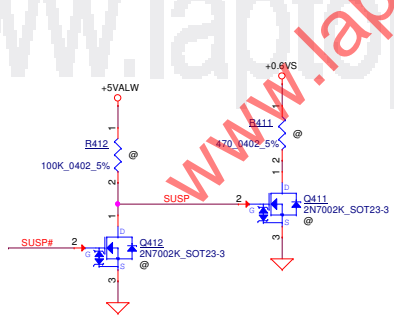


Discharge

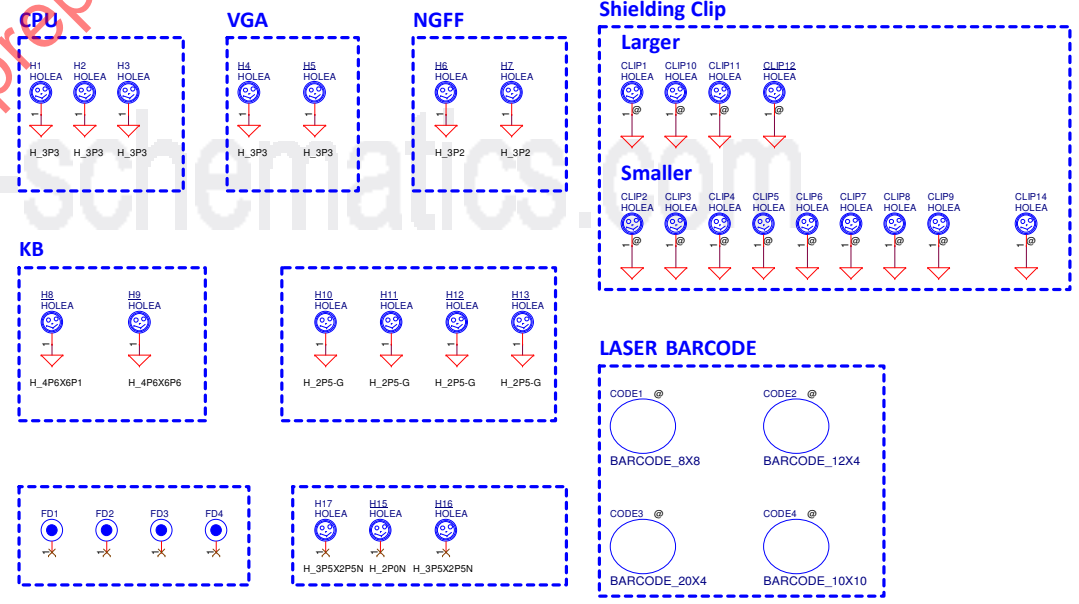
For +1.8VALW Discharge



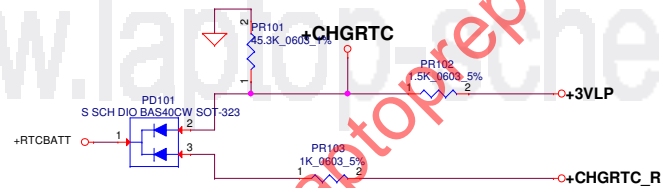
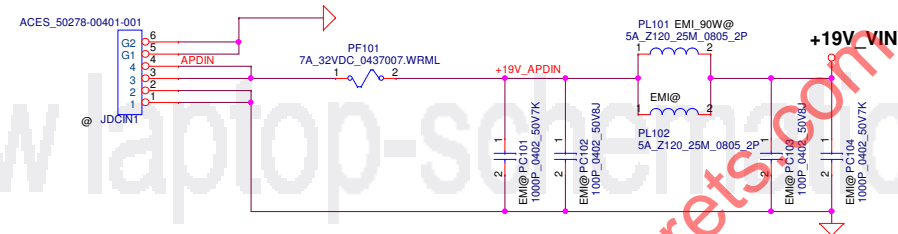
For +0.6VS Discharge



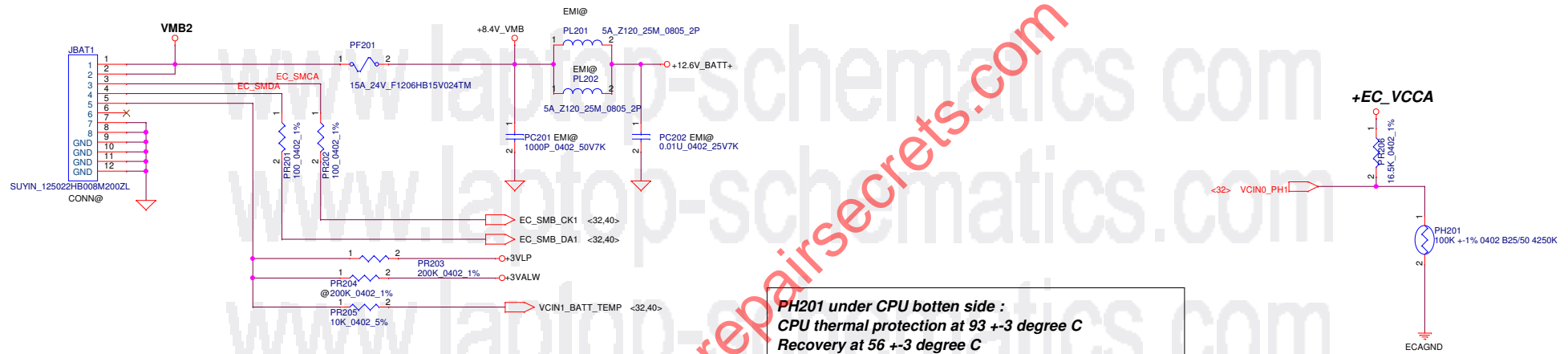
Screw Hold



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				Custom	2A
				Date:	Wednesday, June 21, 2017
				Sheet	37 of 51

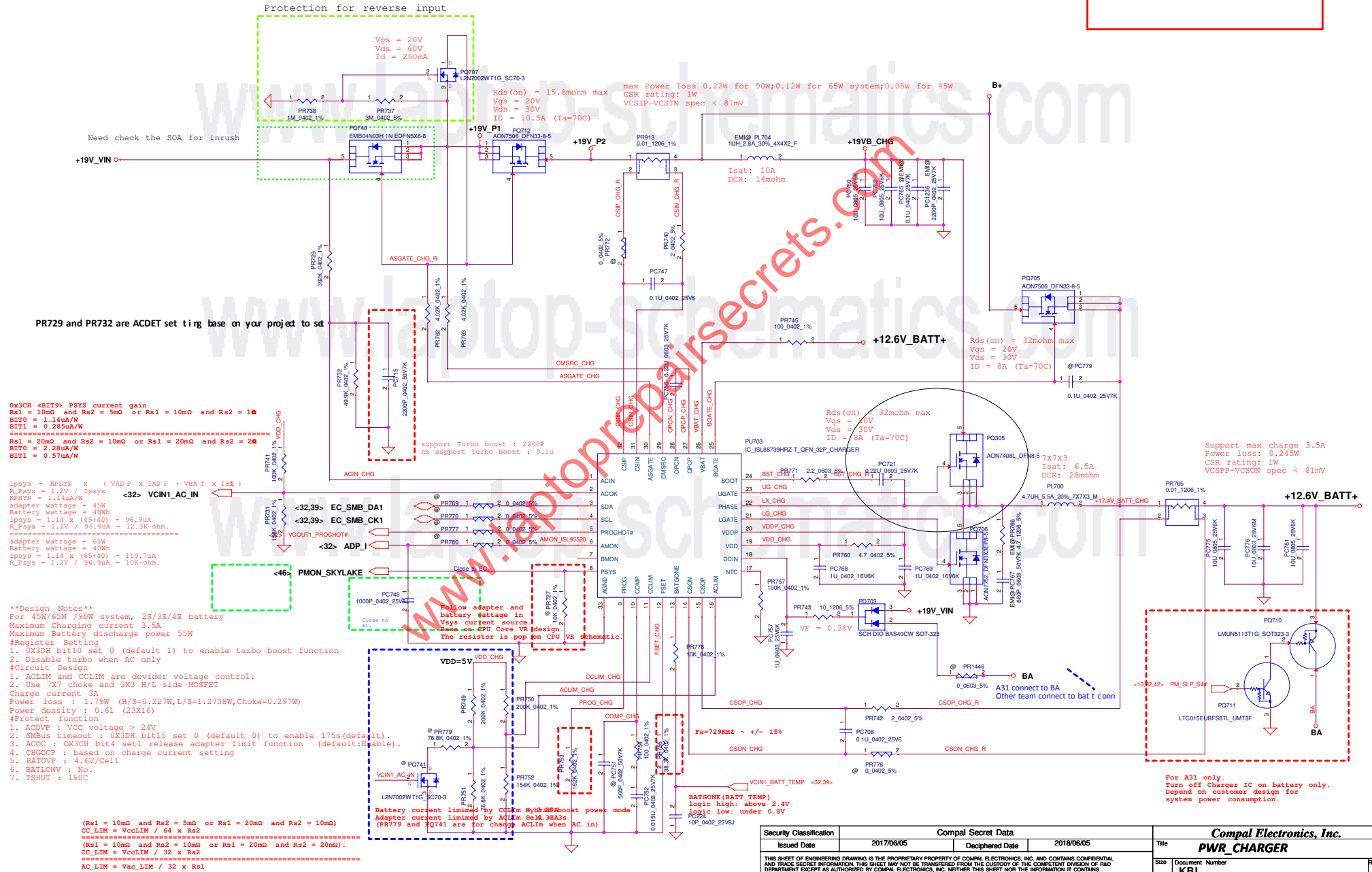


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				Date: Wednesday, June 21, 2017		Sheet 38 of 38

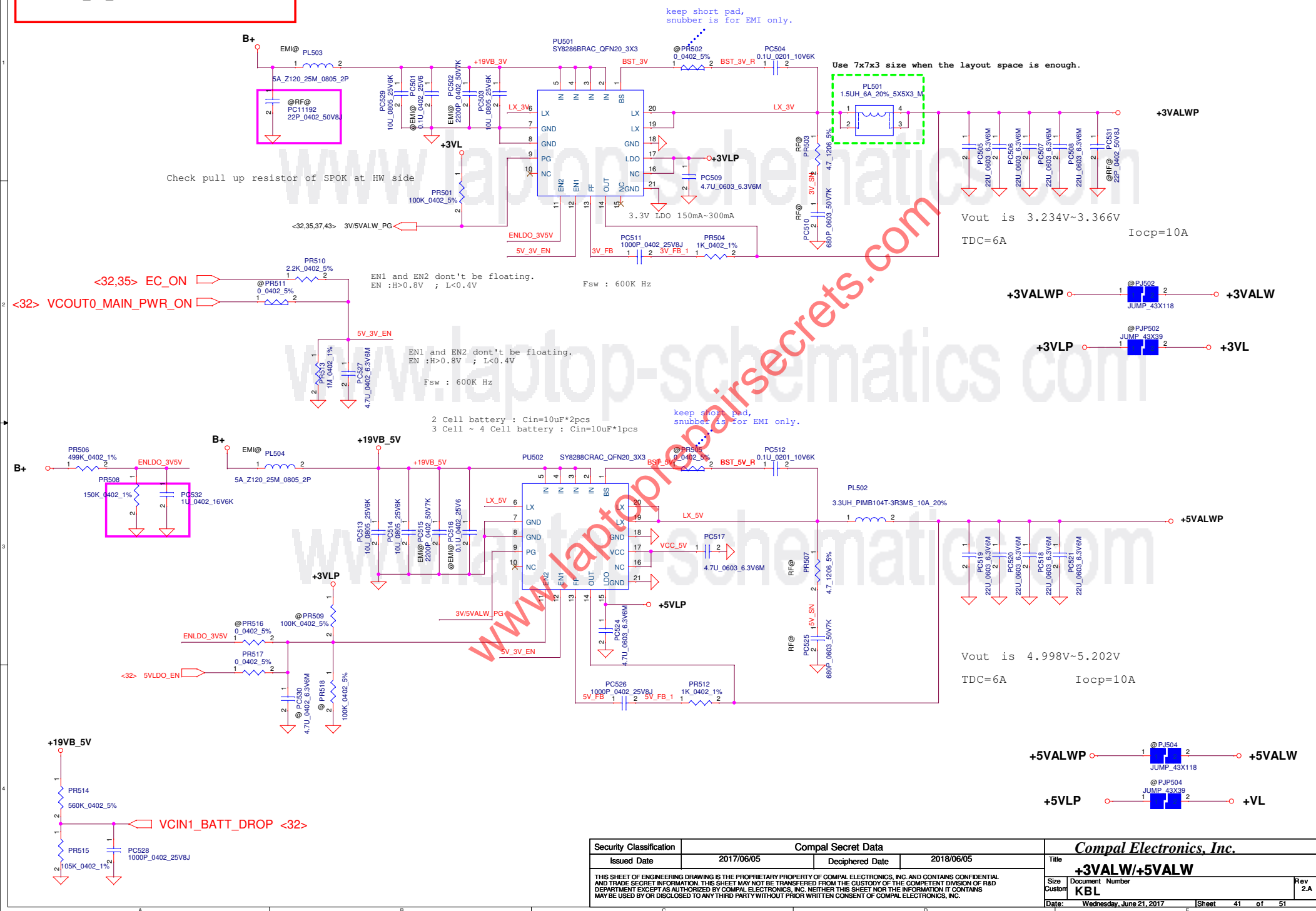


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				Date: Wednesday, June 21, 2017	Rev 2.A
				Sheet 39 of 51	

Module model information  
ISL95520\_Hybrid\_Boost\_V2.mdd



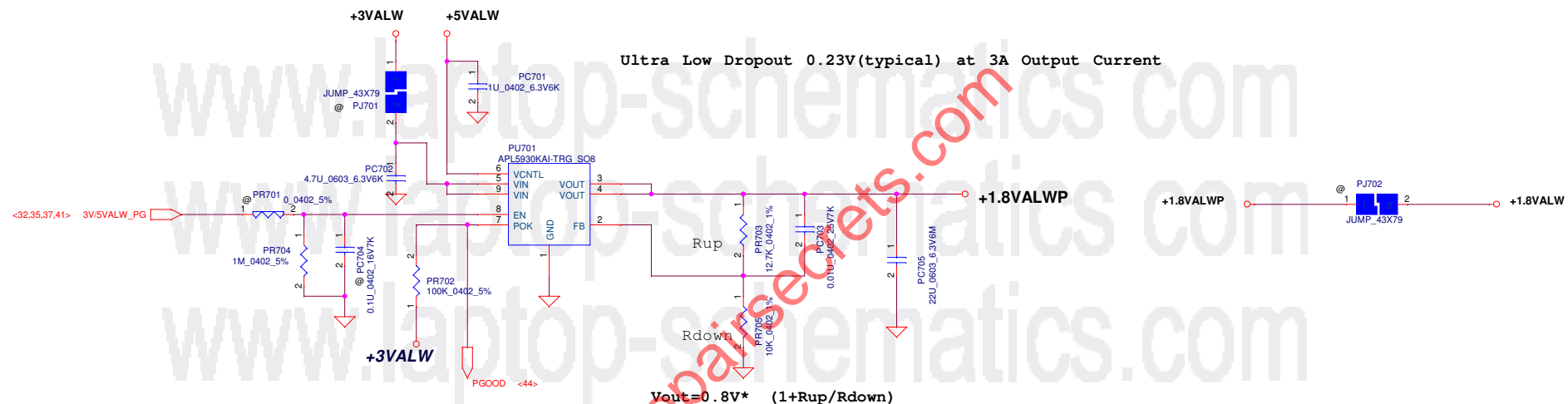
SY8286B\_V3\_single.mdd  
SY8286B\_V3\_dual.mdd





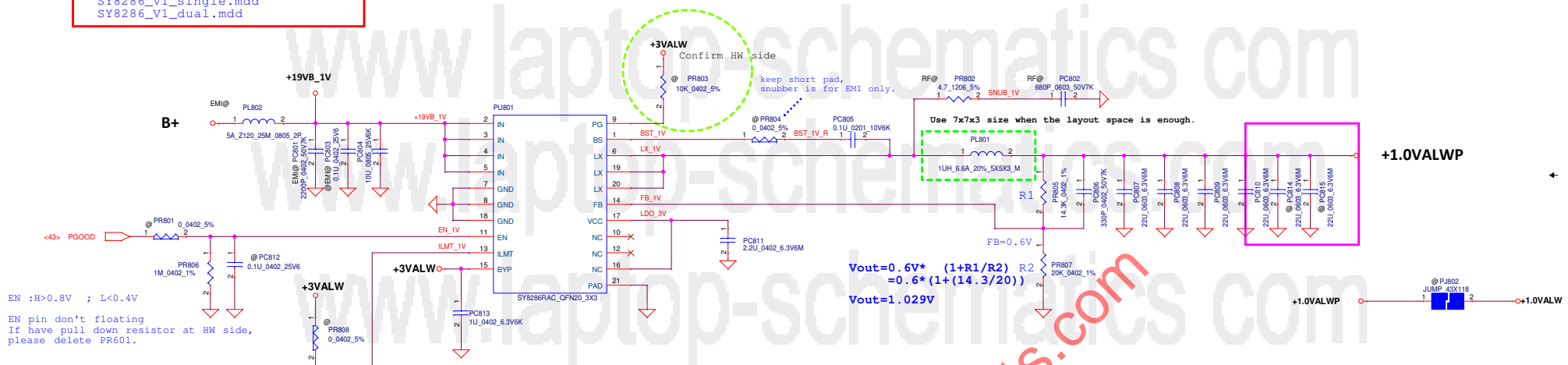
# Module model information

APL5930\_V2.mdd



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Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	APL5930
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				Date: Wednesday, June 21, 2017	Sheet 43 of 51

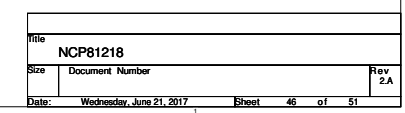
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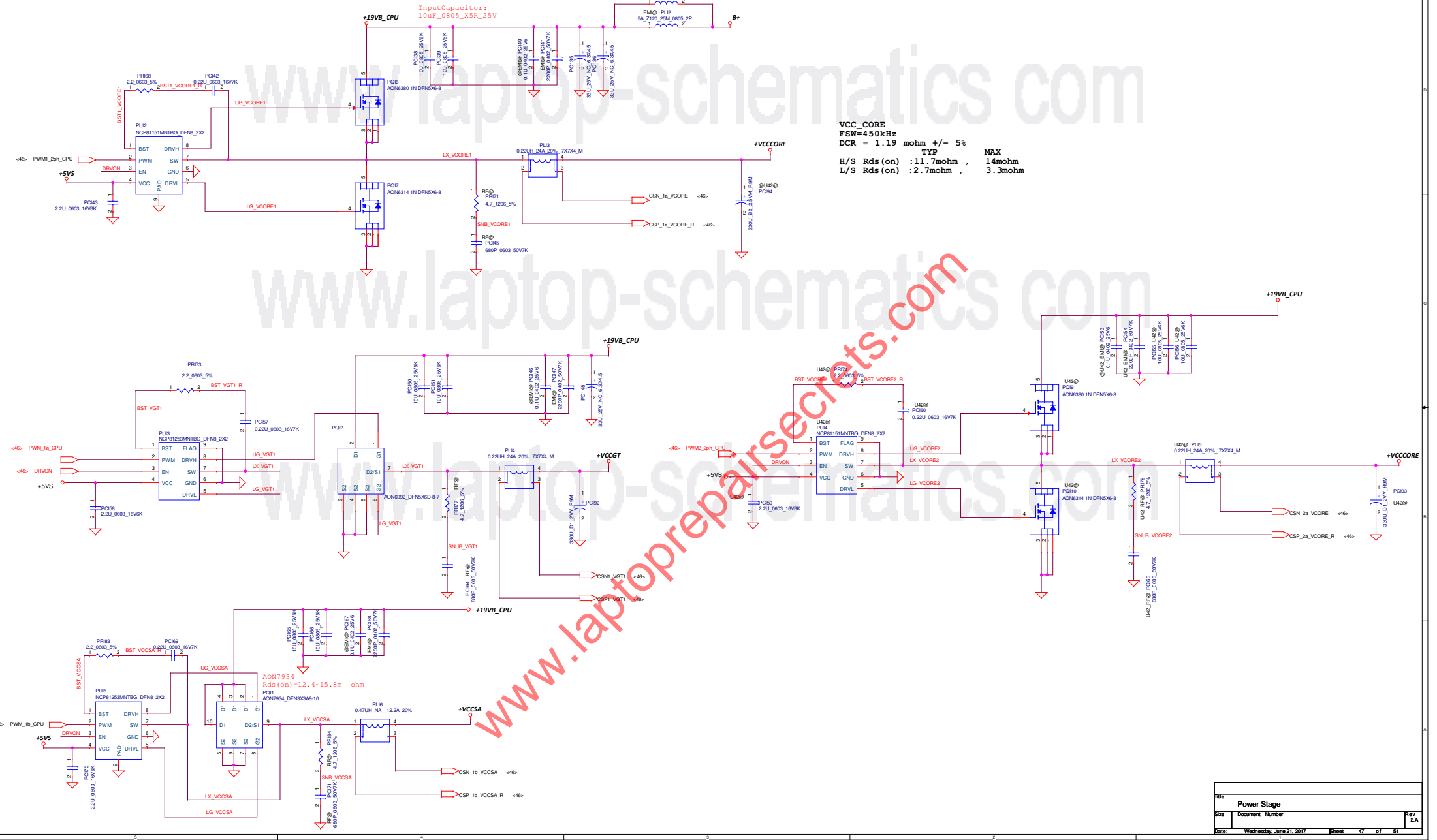
The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

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						Document Number				
						Rev 2A				
						C				
						KBL				
						Date: Wednesday, June 21, 2017				
						Sheet 44 of 51				





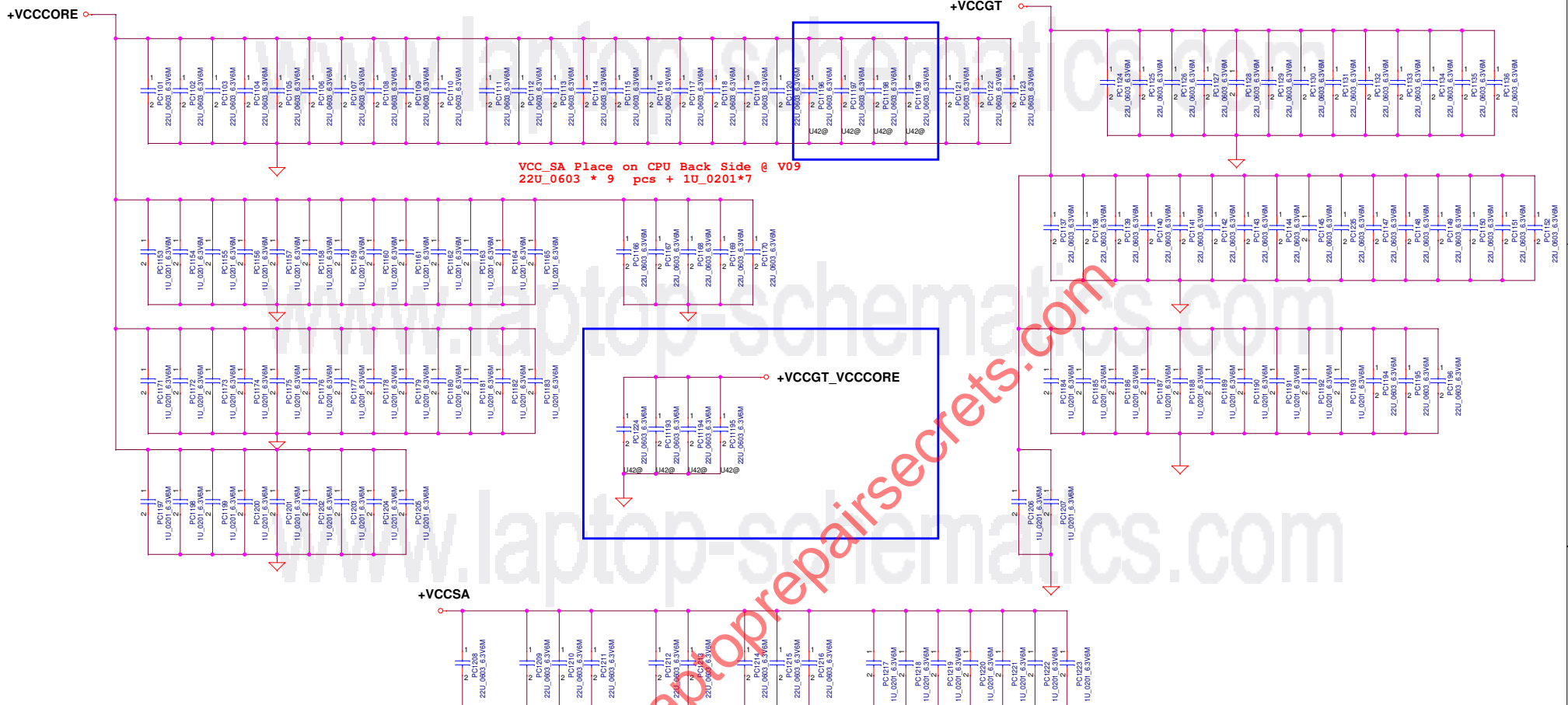
CPU POWER STAGES



Rev	Power Stage	
Doc	Document Number	Rev 2.0
Date	Wednesday, June 21, 2017	Sheet 47 of 51

VCC\_CORE Place on CPU Back Side @ V09  
22U\_0603 \* 36pcs +1U\_0201\*35 pcs

VCC\_GT Place on CPU Back Side @ V09  
22U\_0603 \* 32 pcs +1U\_0201\*12 pcs



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Size	Document Number	Rev		ZA
C	KBL	Date: Wednesday, June 21, 2017		Sheet 48 of 51

PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of voltage steps	96	96	20
Pr8	39K	20K	39K
Pr7	39K	20K	30K
Pr10	1.5K	2K	3K
Pr20	30K	18K	24K
Pr21	1.5K	0	3K
PrC	1.5m	2.7m	1.8m

```
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax
```

VGA@ PR1463 0.0402 1% VGA@ PR1468 1K 0.402 5% Pull high on HW side



+VGA\_CORE  
EDP-Continuous 26.5A  
EDP-Peak 53A  
OCP min 66.4A

**+VGA\_CORE**      Near GPU Core

**+VGA\_CORE** Under GPU Core **GB4-128 package**

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Size	Custom	Document Number	<b>KBL</b>	Rev <b>2A</b>